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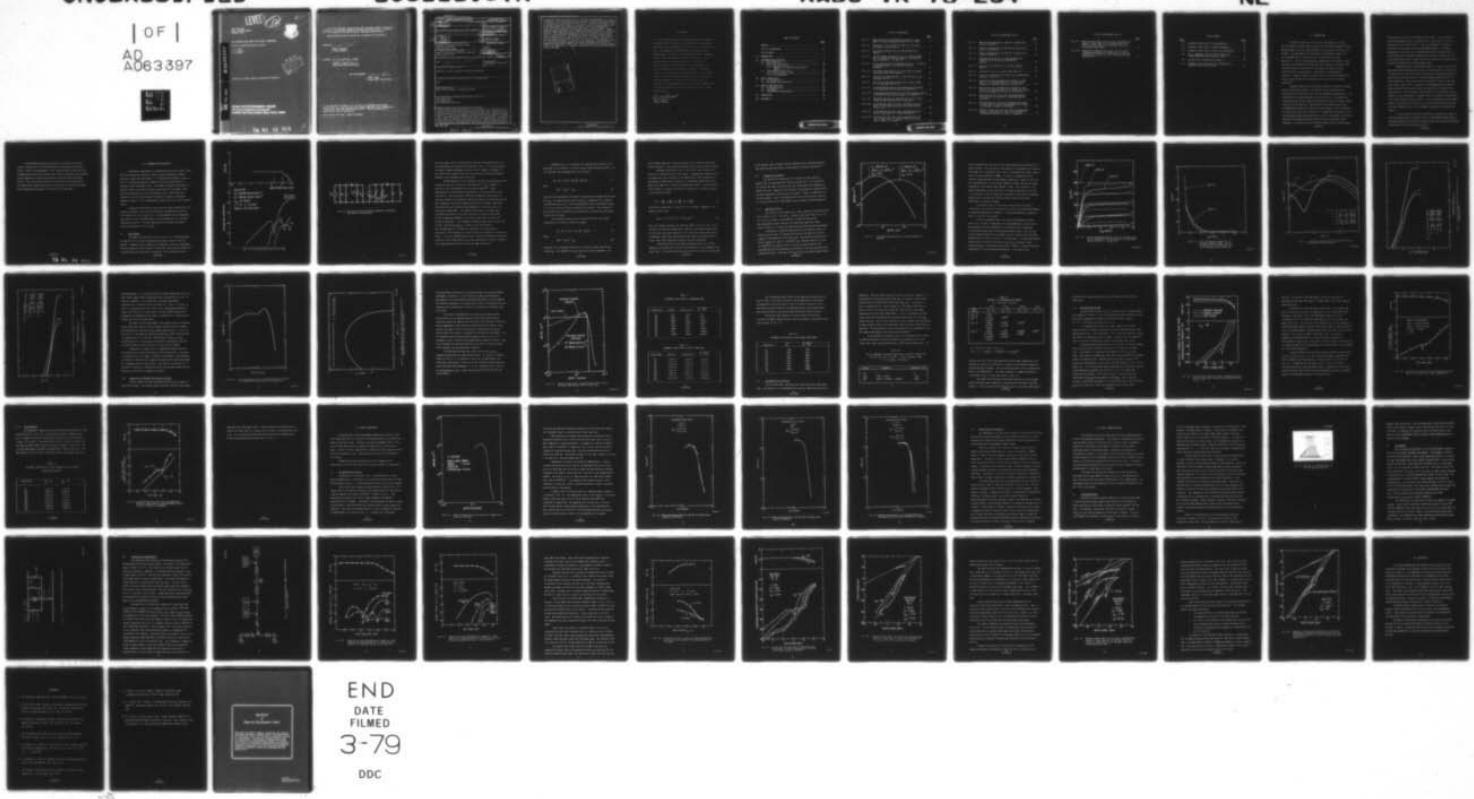

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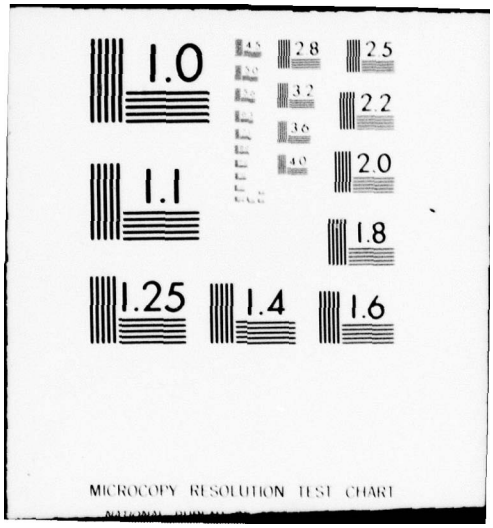
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RADC-TR-78-254
Final Technical Report
November 1978

ION IMPLANTED GaAs POWER FIELD EFFECT TRANSISTORS

Rockwell International Science Center

R. L. Kuvás
J. A. Higgins
D. R. Ch'en

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Tailoring of the doping profile has been shown to be a powerful tool in reducing the intermodulation distortion in GaAs power FETs. Reproducible and uniform preparation of the required sophisticated profiles exceeds the present capability of epitaxial techniques, which has motivated the present investigation of fabricating highly linear power FETs by ion implantation. An analytical device model was developed for exploring the relationship between the active layer profile and the intermodulation distortion. These calculations revealed a complex behavior in the variation of the distortion levels due to partial

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correlation in the contributions due to nonlinear transconductance and output conductance. The device model was used to identify implant doses and energies for approaching an optimum active layer profile. Based on the results, a deep Se implant followed by a shallow Be implant to reduce the doping level close to the surface was used in the device fabrication. The intermodulation distortion of the transistors were measured by the two-tone method. Conventional epitaxial FETs with a flat doping profile were evaluated for comparison purposes. This comparison demonstrated that a 4dB increase in the intercept point for the third order intermodulation product can be realized by using tailored implant profile. The tuning conditions for maximum output power and minimum intermodulation distortion turned out to be virtually identical for the implanted transistors, in contrast to the behavior of conventional devices with flat doping profiles. These performance advantages coupled with the demonstrated high levels of uniformity and reproducibility of doping parameters present ion implantation as a powerful technique in the fabrication of highly linear power FETs.

EVALUATION

1. This Final Report on GaAs Ion Implanted Power FET's represents an 8 month effort to demonstrate the applicability and potential advantages of ion implantation in the fabrication of linear power FET's. The emphasis in the program was on linearity and not maximum power. The results clearly demonstrate that retrograded channels have advantages when linearity is important. An unexpected bonus of retrograde channel profiles has been the observation that the tuning conditions for optimum power and minimum intermodulation distortion are identical. Retrograde channels are a natural for ion implantation. While the retrograde channel can also be obtained by refined control of vapor phase epitaxial growth, it is expected that the simplicity of ion implantation in obtaining this profile will result in higher yields and greater reproducibility, both of which will result in lower production cost.

SVEN A. ROOSILD
Project Engineer

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1.0 INTRODUCTION

The GaAs field effect transistor (FET) has emerged as a highly attractive device in power amplifier applications through the demonstration of multiwatt power levels at X-band frequencies with conversion efficiencies up to 40%.[1] This performance level has generated considerable interest for utilizing GaAs FETs as linear amplifiers in low-distortion system applications. Initial explorations have suggested that the design of linear amplifiers using presently available power FETs presents a challenging task, since the distortion characteristics are complex and separate tuning conditions exist for optimum gain, output power and intermodulation distortion.[2] However, impressive results can be achieved by systematically characterizing the amplifier performance as a function of the loading conditions.[3]

Improved linearity can be achieved by proper tailoring of the doping profile in the active channel. This possibility has been explored by evaluating similar transistors with flat and retrograde doping profiles. The latter profile is characterized by a positive slope, i.e. the doping level increases from the surface towards the substrate followed by an abrupt doping transition at the interface. Some reduction of the measured third order intermodulation products was reported for the retrograde structure compared to the conventional flat profile transistors.[4] Reproducible fabrication of the required sophisticated retrograde profile carries a high degree of difficulty and may well be beyond the present state-of-the-art of epitaxial growth techniques. This observation motivated the present effort to develop highly

linear power FETs based on ion implanted active layers. This approach has yielded unprecedented levels of reproducibility and uniformity in the device characteristics of low-noise FETs.[5] Also, the suitability of implanted transistors in power applications has been demonstrated.[6] In addition, implantation is an ideal tool for reducing the contact resistance and for increasing the drain breakdown voltage by using selective implants to obtain highly doped contact areas. Planar transistor structures can be fabricated by selectively implanting the channel doping as well.

Implantation offers considerable flexibility in profile tailoring by employing multiple implant energies, doses and doping species. Calculations of theoretical profiles were carried out and used in conjunction with device modeling and distortion analysis to identify optimum implant profiles for linear power FETs. These calculations are discussed in Section 2 and show that a deep Se implant with a subsequent shallow compensating Be implant of moderate dose can furnish active layers for power FETs with highly linear characteristics. Other attractive alternatives are to use combined Se and Si implants or even single-dose Si implants, which all can match the performance of an ideal retrograde epitaxial profile. The calculations verify the complex nature of the distortion in GaAs FETs in that correlation effects can cause dips and scalloping effects in the sidetones introduced by intermodulation effects.

A brief outline of the device fabrication is presented in Section 3 including doping profiles resulting from Si, Se and combined Se+Be implants. The contact deposition and pattern definition esentially follow the technology established for fabricating low-noise FETs.[5]

RF measurement procedures and results are discussed in Section 4. The main conclusions of the device modeling are confirmed by the measured results in that a 4 dB improvement in the intercept point for the third order intermodulation product was achieved from a Se+Be implanted FET with optimized profile compared to a conventional epitaxial transistor with flat doping profile. Also, the strong correlation in the sources of nonlinearity was confirmed by the frequent observations of sharp dips in the third and higher order intermodulation products as functions of the input power.

2.0 INTERMODULATION DISTORTION

Experimental measurements of intermodulation distortion (IMD) in GaAs FETs[2] show significant departures from the expected theoretical behavior based on a simple cubic nonlinearity.[7] A representative example is given in Fig. 2-1 and shows pronounced scalloping in the various IMD products as functions of the input power level. This behavior indicates the presence of multiple sources of nonlinearity which can be partially correlated. More extensive experimental results are presented in Sec. 4 and confirm the complexity of the nonlinear behavior of GaAs FETs leading to unexpected asymptotic behavior of the intermodulation products and also to gain expansion effects.

A thorough understanding of the origins of these characteristics are required to design a transistor with minimized intermodulation distortion. The recognition of this problem led to a strong emphasis on device modeling and analysis of resulting IMD products to provide guidelines for optimized implantation profiles. The device model and the calculated performance results are presented in this section.

2.1 Device Model

The simplified equivalent circuit in Fig. 2-2 of a tuned GaAs power FET amplifier will be used to highlight the primary sources of nonlinear behavior. Feedback effects (common source impedance, drain-gate capacitance) have been neglected in the interest of simplicity, since these are expected to introduce only minor quantitative corrections in the calculated results.

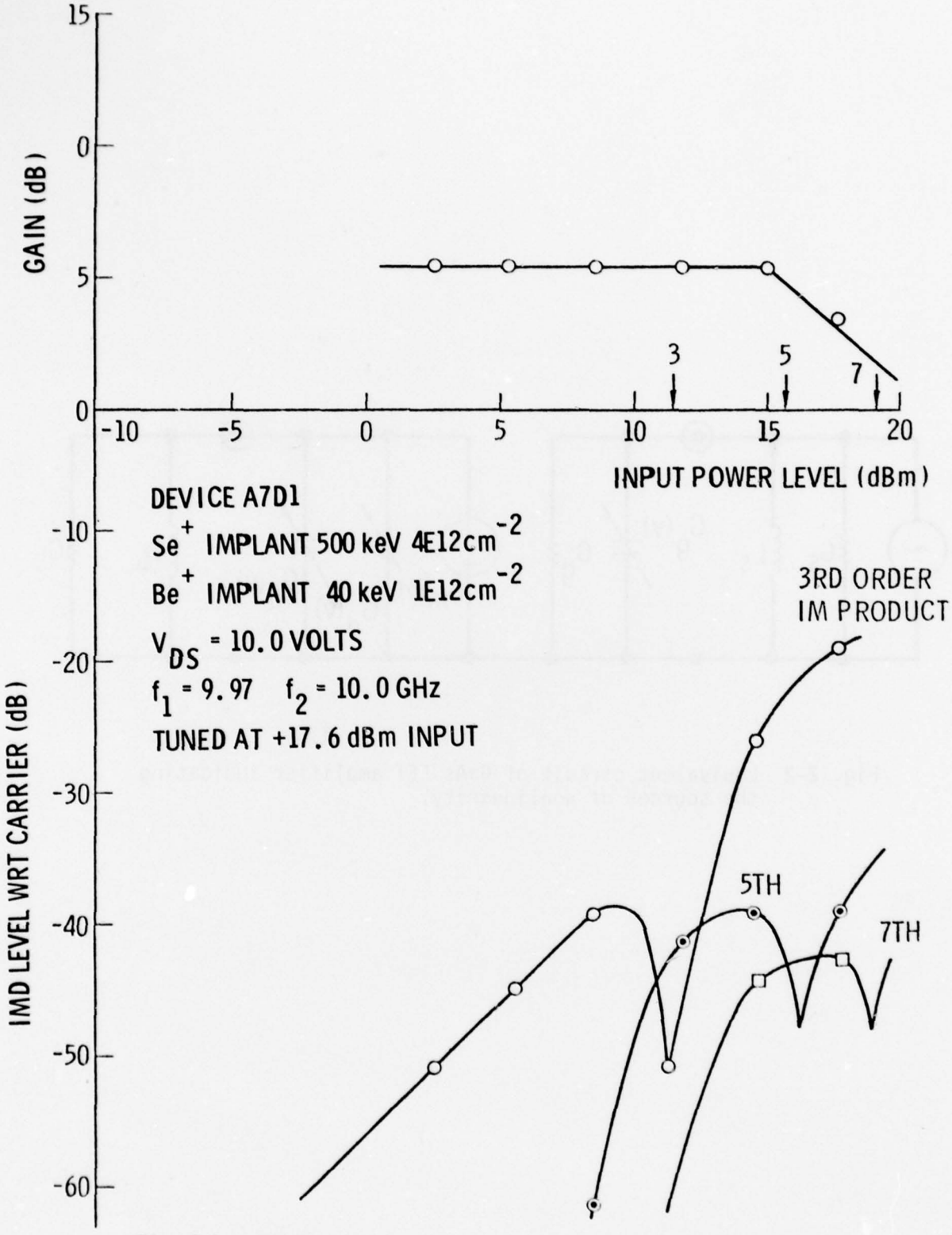

Fig. 2-1 Measured gain and intermodulation products vs input power for Se+Be implanted GaAs power FET at 10 GHz.

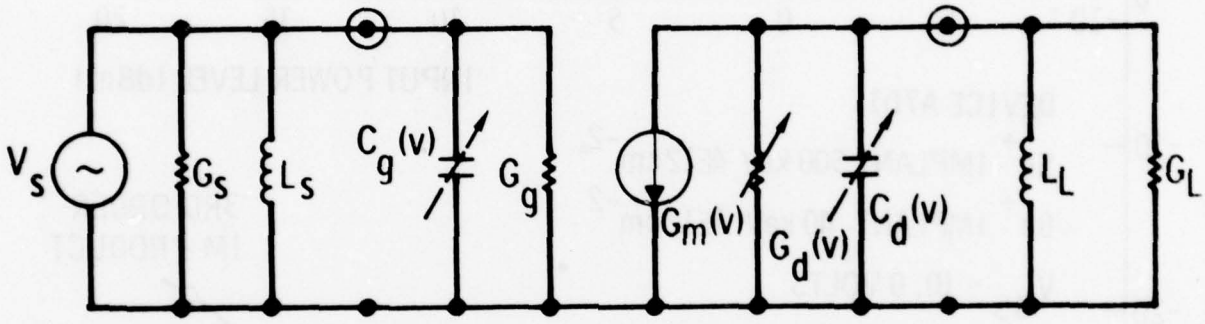

Fig. 2-2 Equivalent circuit of GaAs FET amplifier indicating the sources of nonlinearity.

Also, the input circuit of the transistor has been transformed from a series RC representation to an equivalent GC parallel circuit. This transformation introduces frequency dependence in the GC circuit elements, although it is well justified to consider them to be constant within the narrow bandwidth assumed in the intermodulation calculations.

The nonlinearities in the response of the FET can be accounted for by introducing realistic variations in the equivalent circuit elements as functions of the instantaneous drain and gate voltages.[8,9] A good approximation of these functional dependencies can be obtained from static calculations. Such calculations show that the dominant contributions to nonlinear response can be expected from the variation in transconductance with gate voltage and in the drain conductance with drain voltage. Additional contributions arise from the voltage dependencies in the gate-source and drain-source capacitances. The simplifications made in our model have eliminated any effects of the input capacitance variation on the output current through the assumption of an ideal voltage source V_s across this nonlinear capacitance. This assumption introduces small errors in the limit of small input losses $G_g/\omega C_g \ll 1$, which is well satisfied for a well-designed GaAs FET. The physical mechanism for a varying drain capacitance is the formation of a dipole region in the channel at large drain biases. It will be assumed that the static capacitance between the source and the drain is much larger than this variable contribution, so that a constant drain capacitance may be used in the actual IMD calculations.

Mathematically, it is convenient to represent the variation in the equivalent circuit elements in a Taylor series around the operating point. By this approach, the transconductance can be written,

$$G_m = G_{m1} + G_{m2} V_g + G_{m3} V_g^2 + G_{m4} V_g^3 + \ldots\ldots \quad (1)$$

where

$$V_g(t) = V_{gs}(t) - V_{go} \quad (2)$$

specifies the instantaneous deviation of the gate-source voltage from the gate bias V_{go}. In determining the coefficients G_m, a polynomial fit is made to the calculated variation in the transconductance from a forward gate voltage of 0.5 V to a reverse voltage corresponding to pinchoff. The variation in G_m with drain bias is neglected by averaging this variation over the typical range of drain voltages.

A corresponding expression can be written for the drain output conductance as a function of the drain voltage

$$G_d = G_{d1} + G_{d2} V_d + G_{d3} V_g^2 + G_{d4} V_d^3 + \ldots\ldots \quad (3)$$

where

$$V_d(t) = V_{ds}(t) - V_{do} \quad (4)$$

represents the instantaneous deviation in the drain voltage from the bias voltage V_{do}. The dependence of G_d on gate bias has been neglected. The

drain voltage range used in the calculation of the expansion coefficients extends from half of the saturation voltage to twice the drain bias voltage.

Analogous expressions to Eqs.(1)-(4) can be used to express the variation in the gate and drain capacitances. Although these nonlinearities are neglected in the calculation of the IMD products, they can provide an explanation of observed gain expansion at intermediate input signal levels when the FET amplifier is tuned for maximum power output. In the presence of an RF voltage, $A = A_1 \sin\omega t$, the effective capacitance is found by expansion of the resulting current:

$$I(t) = C \frac{dA}{dt} = C_1 \frac{dA}{dt} + \frac{1}{2} C_2 \frac{dA^2}{dt} + \frac{1}{3} C_3 \frac{dA^3}{dt} + \ldots\ldots \quad (5)$$

The effective capacitance is given by the first harmonic component of the equation, which yields

$$C_{eff} = C_1 + 0.25\ C_3\ A_1^{\ 2} + 0.125\ C_5 A_1^{\ 4} + \ldots. \quad (6)$$

Thus, the reactance tuning of the input and output circuits in Fig. 2-2 are different for obtaining maximum small-signal gain and maximum output power. For the latter case, gain expansion will be observed in going from small to intermediate signal levels providing that the improving reactance match at larger signal levels dominates the power saturation mechanisms.

A modified version of the model developed by Pucel et al.[10] was employed to calculate the variation in the equivalent circuit parameters with signal level. This modified approach divides the active layer into a maximum

of 150 laminar layers to model realistic doping profiles, and has previously been used with excellent results in the design of low-noise transistors.[5]

2.2 Doping Profile Effects

Tailoring of the doping profile in the active layer provides a powerful tool for optimizing the linearity of power FETs. This subsection will discuss the types of profiles that can be achieved by ion implantation towards this end. Examples will be given of resulting device characteristics, and their dependence on gate and drain voltages. Finally, a comparison will be given between a typical implanted profile and possible epitaxial profiles to illustrate the relative performance levels available by these approaches.

2.2.1 Implanted Profiles

The available n-type dopant ions in GaAs suitable for fabricating FET active layers are Si, S, Se and Te. The most promising of these are Si and Se, since S has shown a strong tendency to outdiffuse during the post-implantation anneal leading to an undesirable negatively sloped profile,[5] while Te is a heavy ion requiring quite high accelerating energies.

Single-dose Se implants have proven to be an excellent choice for preparing active layers of low-noise FETs and will be used as an initial example for the purposes of this discussion. Calculated distributions of a 200 keV implant at a dose of $3.1 \times 10^{12} cm^{-2}$ and a 500 keV implant at a dose of $2.6 \times 10^{12} cm^{-2}$ are shown in Fig. 2-3 using LSS range statistics and experimentally derived information on diffusion of the ions during the post implantation anneal. Both these profiles provide a desirable peaked feature,

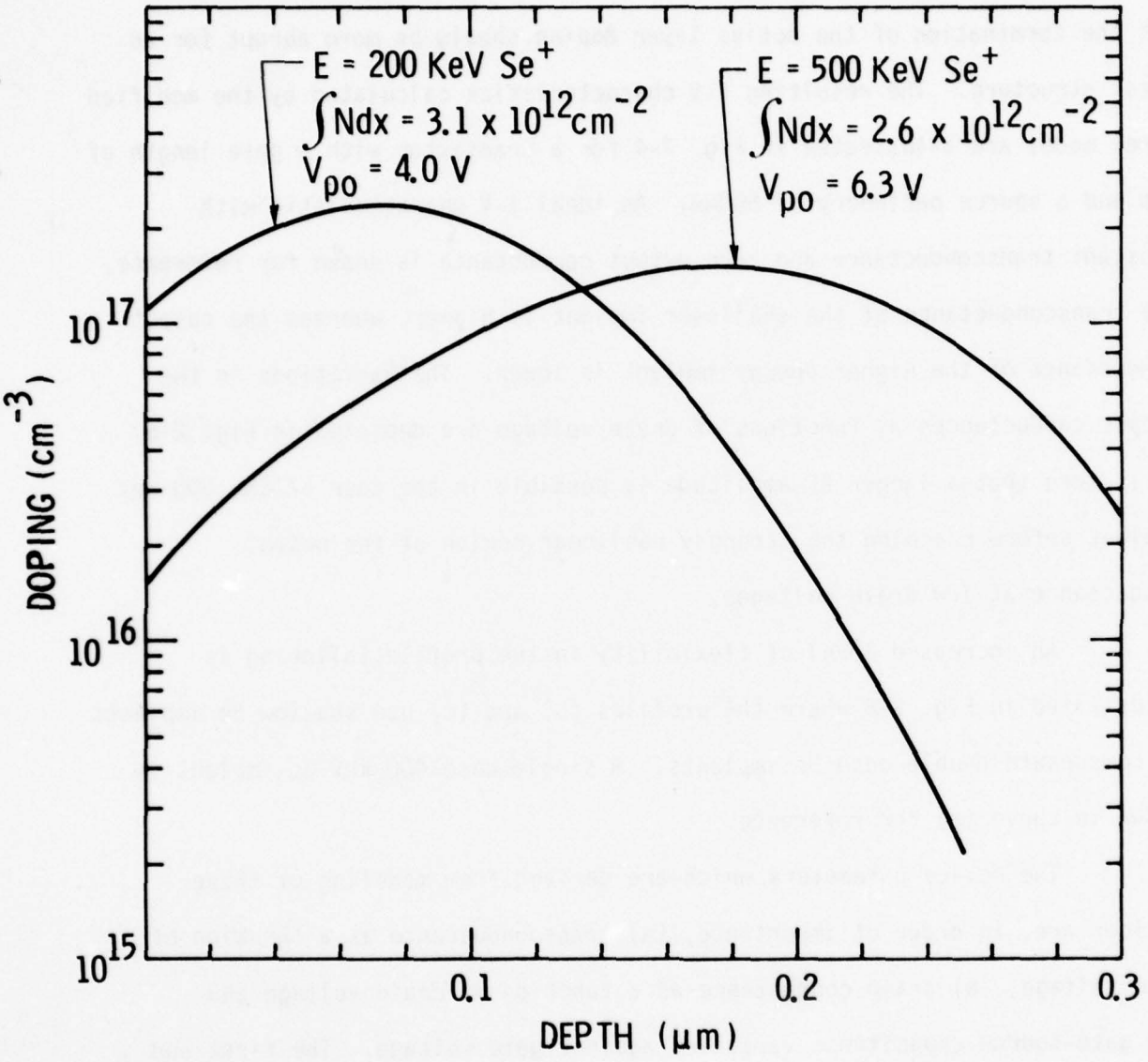

Fig. 2-3 Calculated doping profiles for 200 and 500 keV Se implants.

but the termination of the active layer doping should be more abrupt for an ideal structure. The resulting I-V characteristics calculated by the modified Pucel model are illustrated in Fig. 2-4 for a transistor with a gate length of 1μm and a source periphery of 500μm. An ideal I-V characteristic with constant transconductance and zero output conductance is shown for reference. The transconductance of the shallower implant is higher, whereas the output conductance of the higher energy implant is lower. The variations in the output conductances as functions of drain voltage are depicted in Fig. 2-5. It is seen that a larger RF amplitude is possible in the case of the 500 keV implant before reaching the strongly nonlinear region of the output conductance at low drain voltages.

An increased level of flexibility in the profile tailoring is illustrated in Fig. 2-6 where the profiles (b) and (c) use shallow Be implants to compensate double-dose Se implants. A single dose 400 keV Se implant is shown in curve (a) for reference.

The device parameters which are derived from modeling of these devices are, in order of importance, (a) transconductance as a function of gate voltage, (b) drain conductance as a function of drain voltage and (c) gate-source capacitance variation against gate voltage. The first and third of these characteristics are shown in Figs. 2-7 and 2-8 for the three implanted profiles given in Fig. 2-6. In both cases, it is seen that improved characteristics in terms of variation of g_m and C_{gs} and range of gate voltage available, are obtained for profile (c); that is, a profile featuring a deep peak of the net implanted distribution. In the case of the

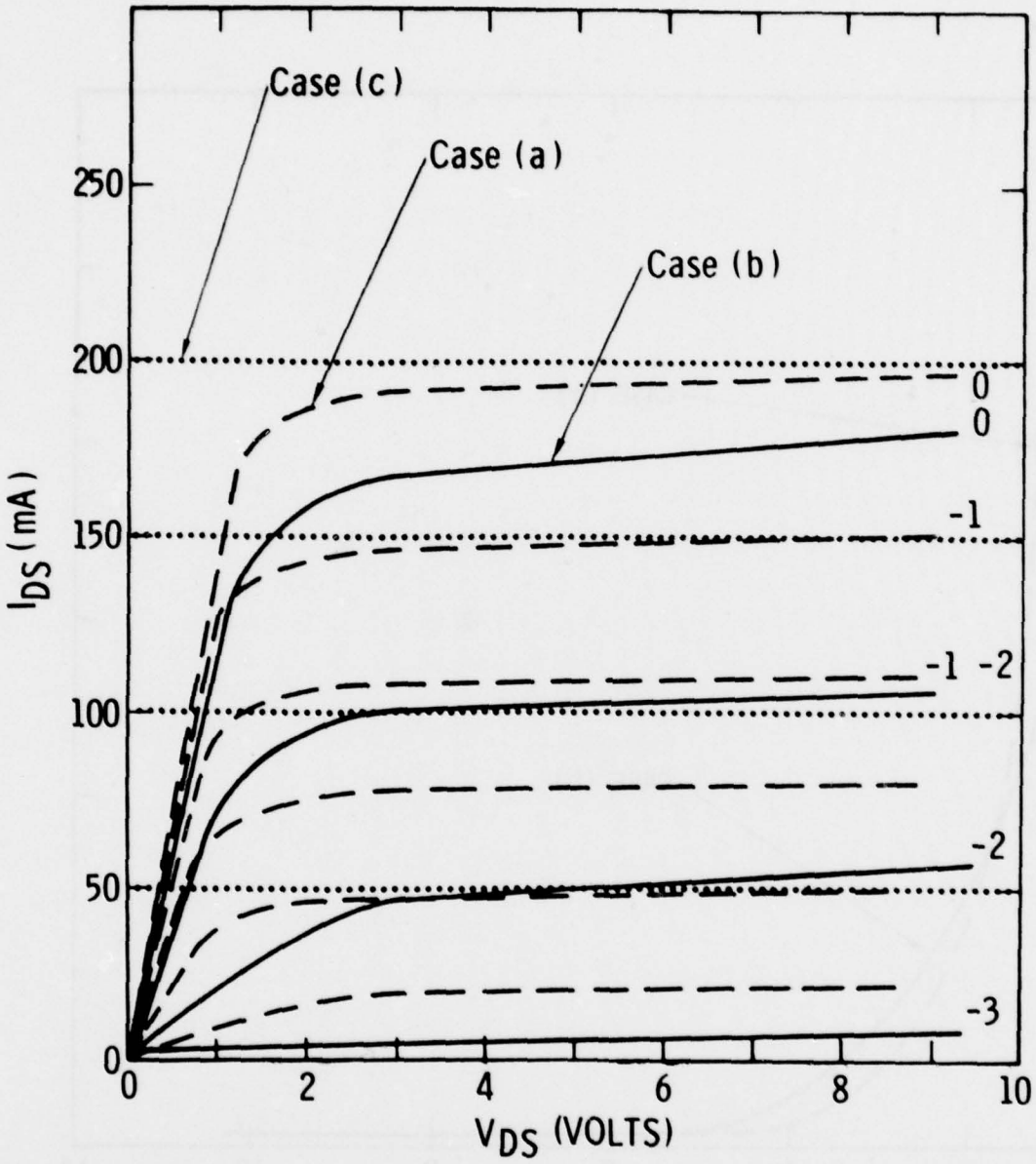

Fig. 2-4 Current-voltage characteristics of ion implanted GaAs FETs (a) 500 keV Se implant $3 \times 10^{12} cm^{-2}$ (b) 200 keV Se implant $4 \times 10^{12} cm^{-2}$ (c) Ideal FET.

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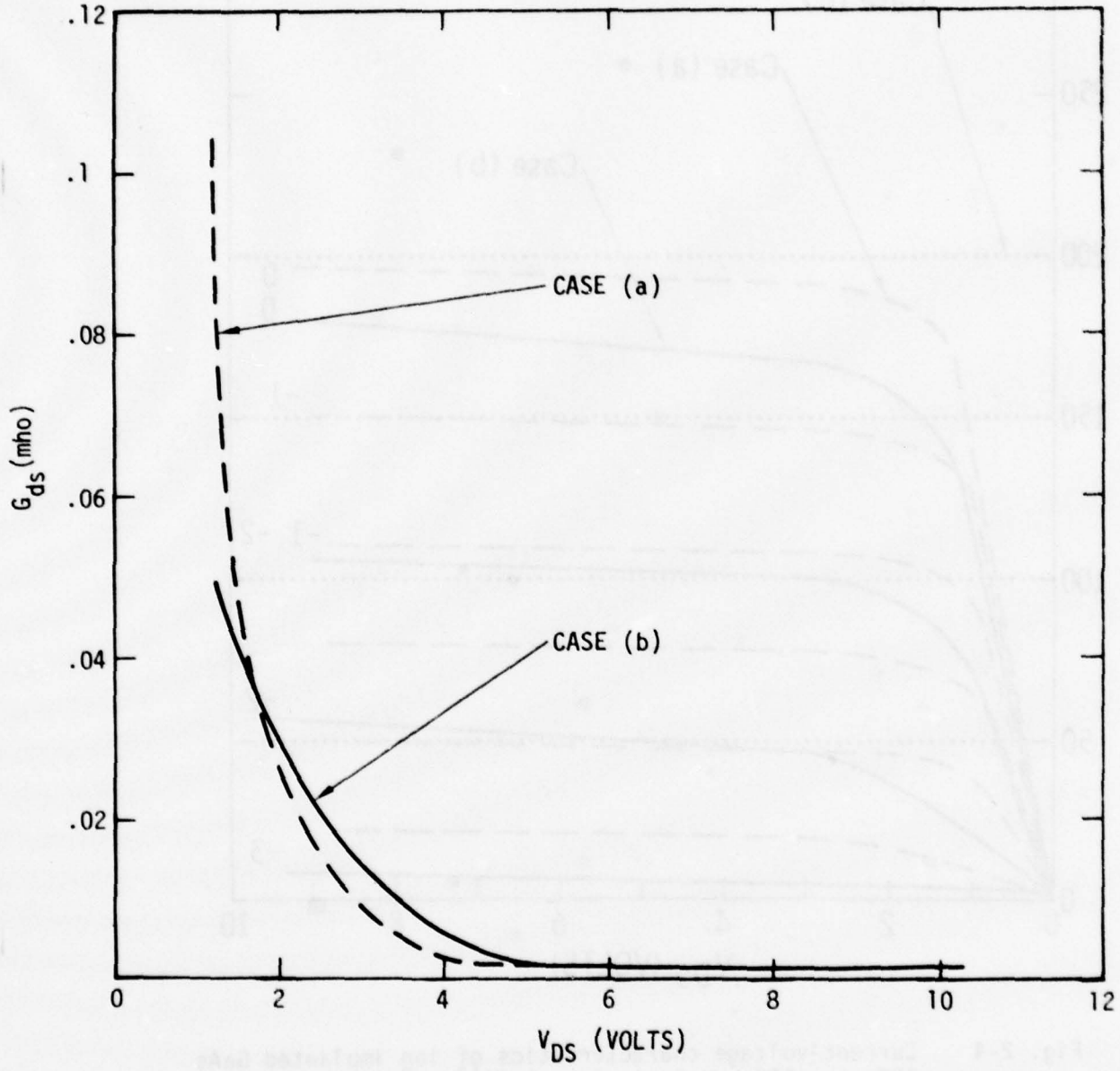

Figure 2-5 Drain conductance of GaAs FETs of different implant energy. Case (a) for 500 keV Se^+ at $3x10^{12}/cm^2$. Case (b) for 200 keV Se^+ at $4x10^{12}/cm^2$.

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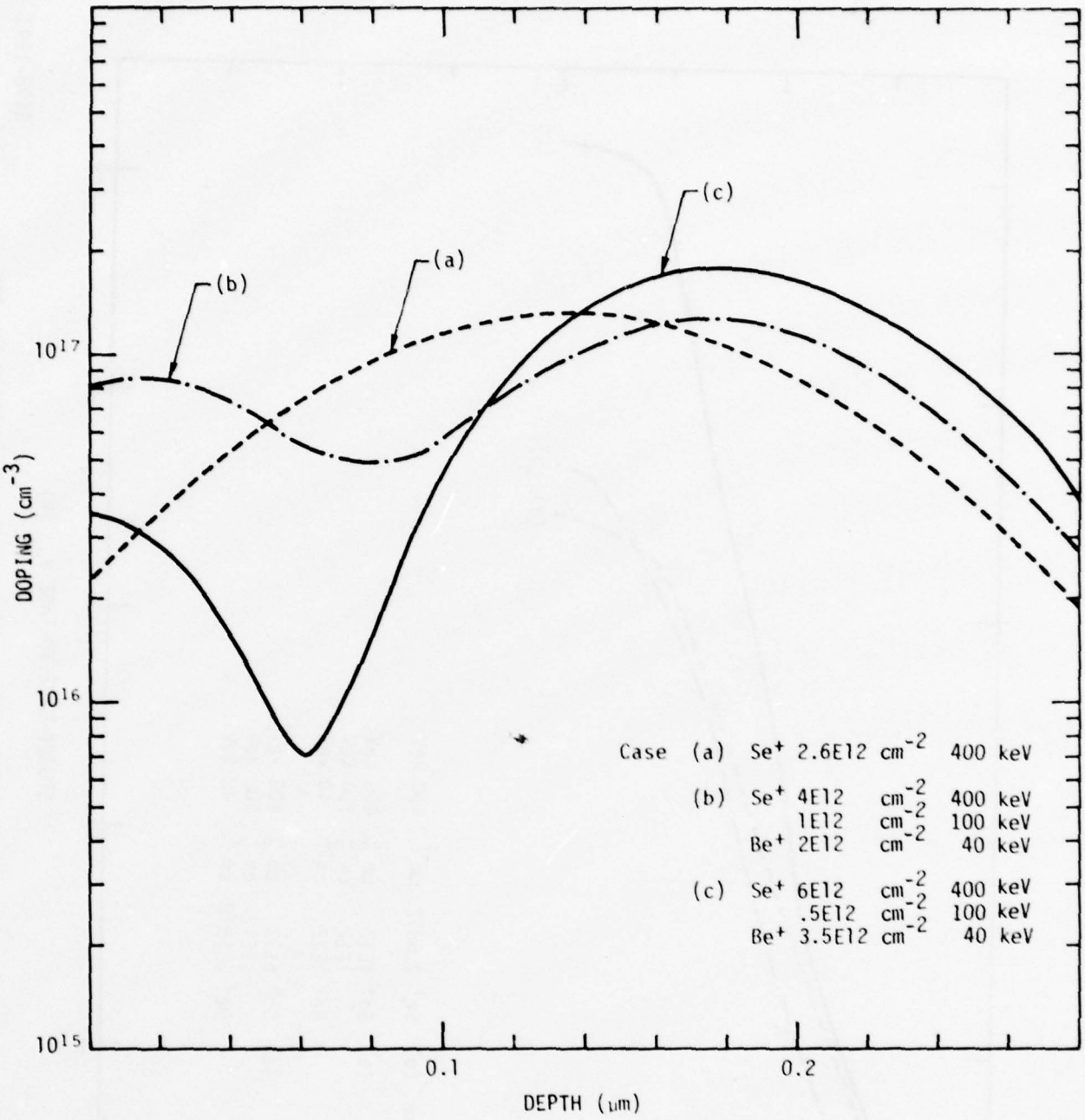

Fig. 2-6 Calculated doping profiles for single-dose Se implant and multiple dose Se+Be implants.

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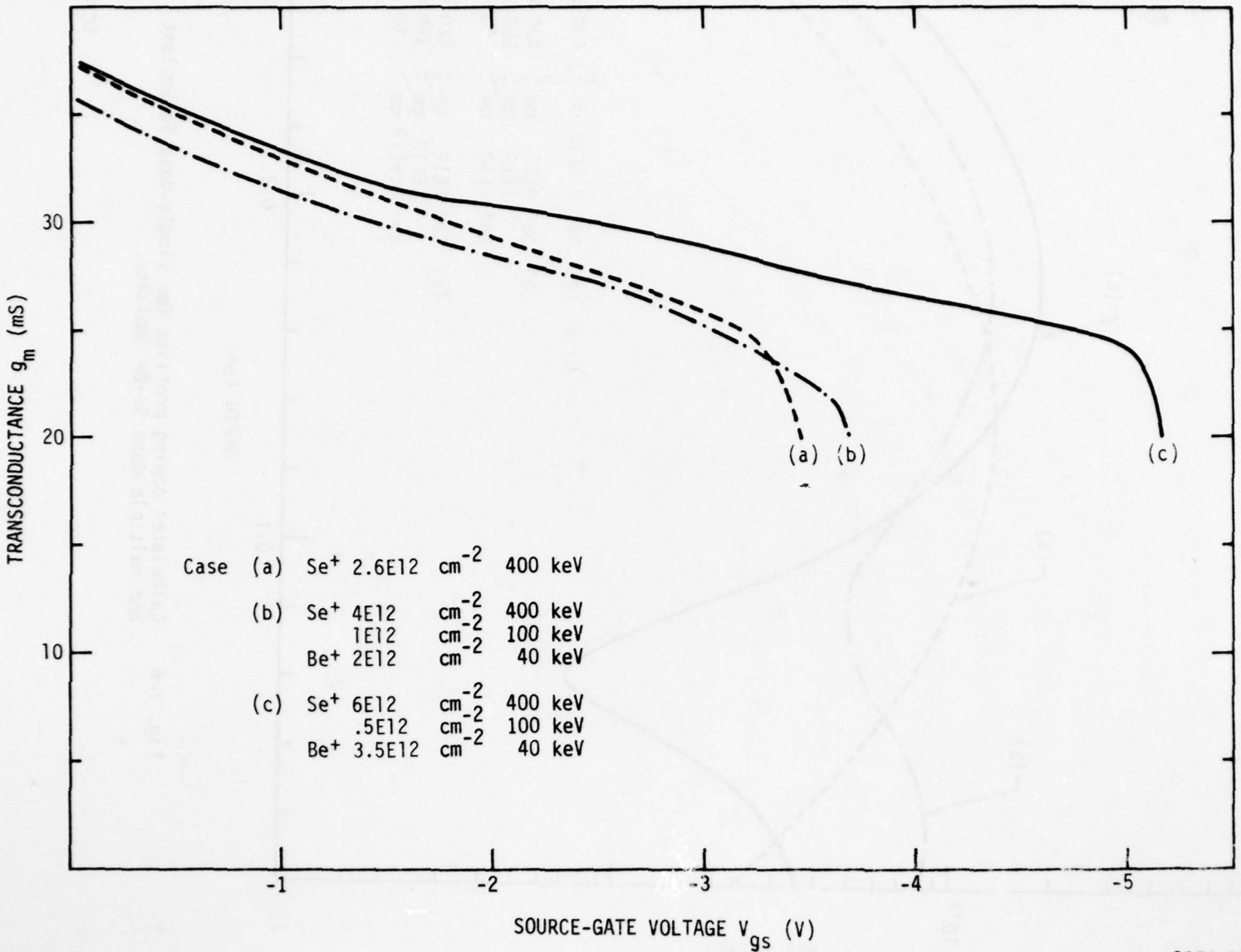

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Fig. 2-7 Variation in transconductance vs gate voltage for ion implanted GaAs FETs.

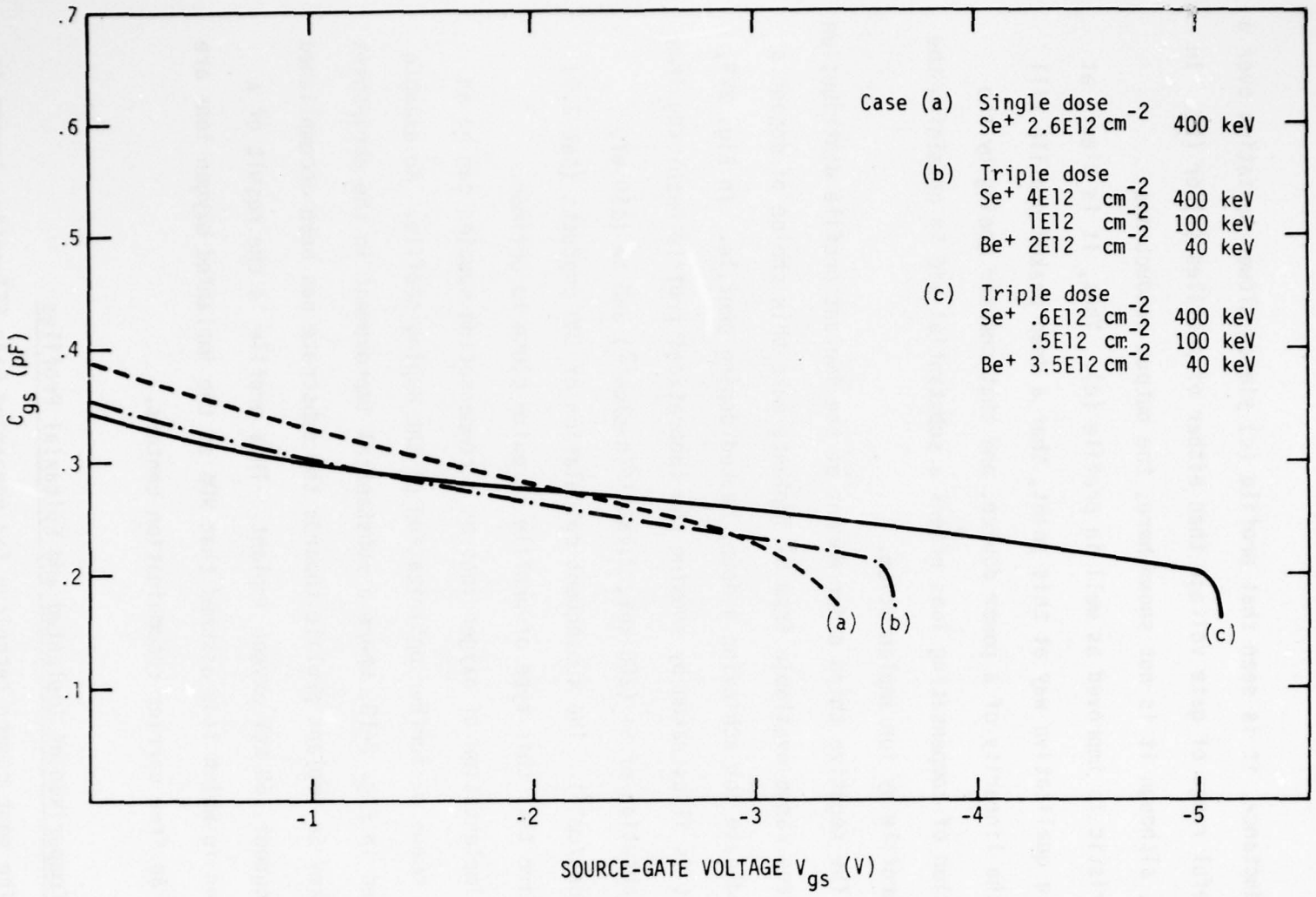

Fig. 2-8 Variation in gate-source capacitance vs gate voltage for ion implanted GaAs FETs.

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transconductance, it is seen that profile (c) yields slower variation over a wider useful range of gate voltage than either of profiles (a) or (b). In addition, although it is not shown here, the output conductance characteristic is improved as well in profile (c). Thus, it is clear, at least in a qualitative way at this point, that a deep peaked profile will improve the linearity of a power device, and that counter doping by the introduction of compensating ions offers a substantial aid in obtaining the optimum profile by ion implantation.

The negative third order moment of the implant profile distribution and the deep range available from Si implants make this choice of dopant a prime candidate for achieving a deep, peaked doping profile. In Fig. 2-9, this point is illustrated by showing the theoretical profile resulting from a co-implantation of Si (200 keV, 2.7×10^{12} ions/cm^{-2}) and Se (110 eV, 0.7×10^{12} ions/cm^{-2}). The subsequent calculation of IMD products (Sec 2.3) will confirm that this type of profile is quite close to optimum.

Implantation of oxygen ions as a compensating species can be an efficient means of further optimization of the doping profile. An example is provided in Fig. 2-10, where a substantial improvement in the abruptness of a 400 keV Se implant profile towards the substrate has been accomplished by a subsequent 160 keV oxygen implant. This profile is the result of a calculation in which itis assumed that 90% of the implanted oxygen ions are effective as free carrier recombination centers.

2.2.2 Comparison of Implanted and Epitaxial Profiles

The most common technique for preparing GaAs FET active layers is vapor phase epitaxy. This approach offers excellent flexibility with regard

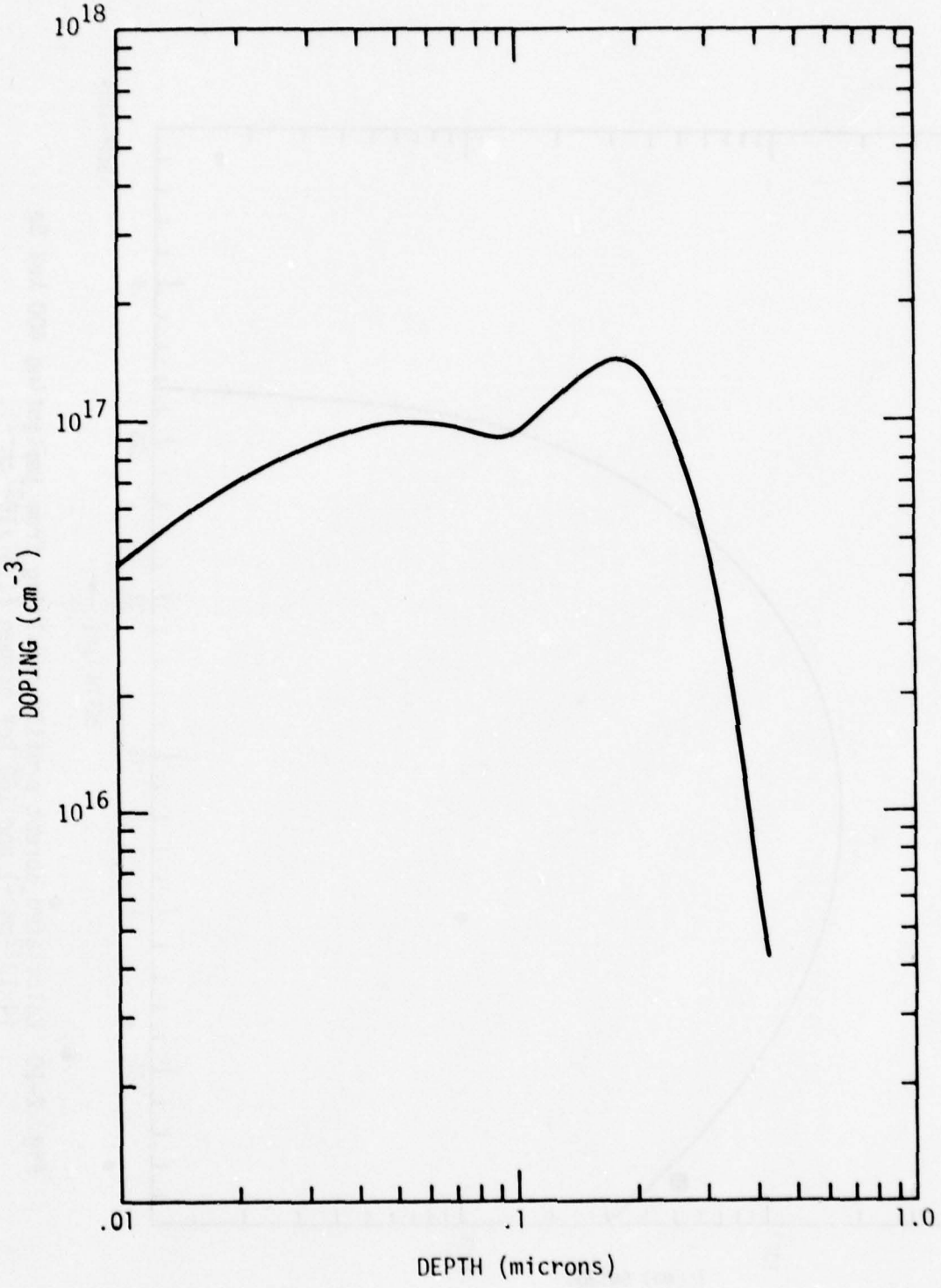

Fig. 2-9 Calculated doping profile from implantation of 200 keV Si ($2.7 \times 10^{12} cm^{-2}$) and 110 keV Se ($0.7 \times 10^{12} cm^{-2}$).

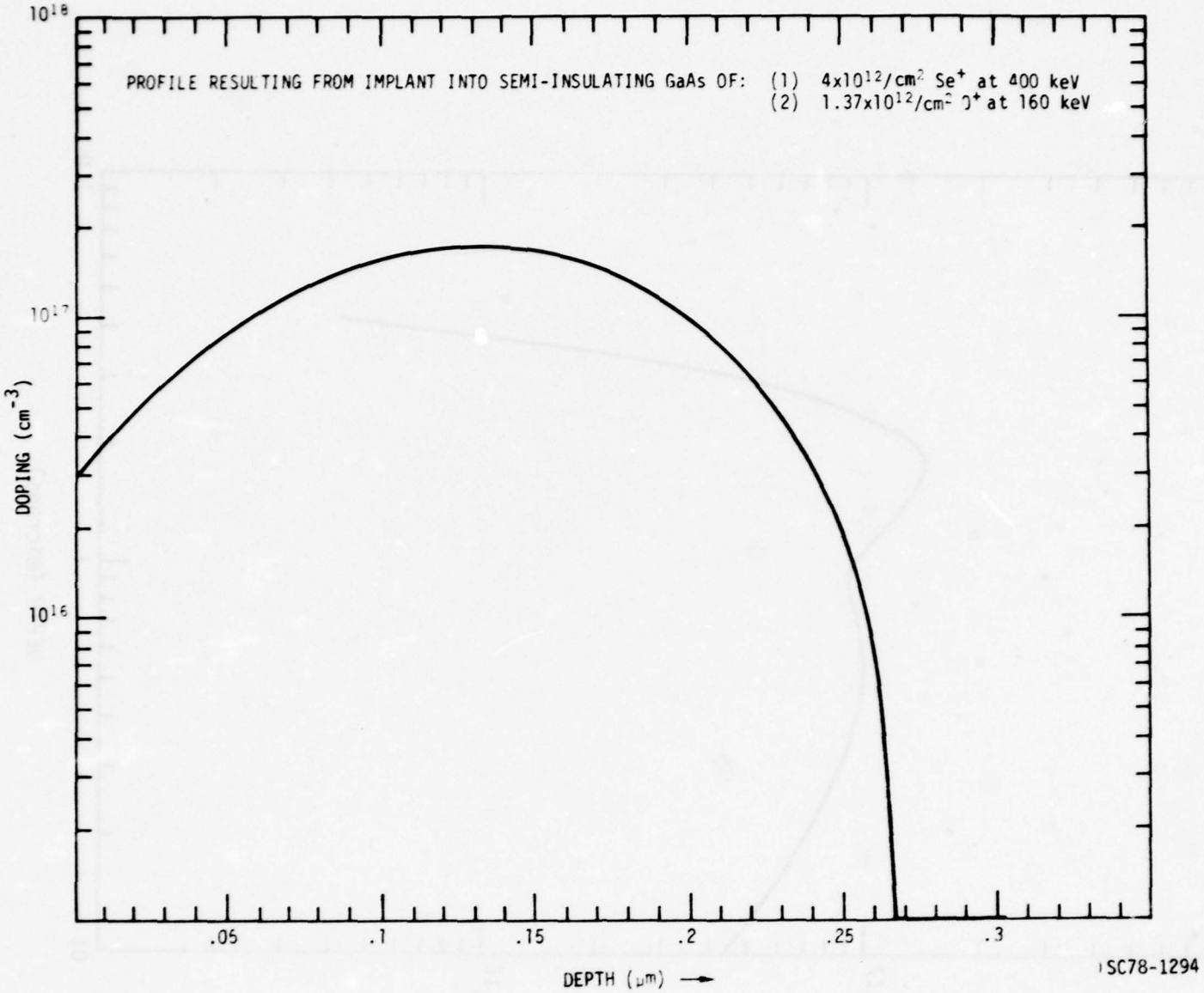

Fig. 2-10 Calculated abrupt profile resulting from implanting 400 keV Se ($4x10^{12}cm^{-2}$) and 160 keV oxygen ($1.37x10^{12}cm^{-2}$).

to doping profile tailoring, and has provided power FETs with outstanding performance. Therefore, it is of interest to compare the theoretical performance of FETs with implanted and epitaxial profiles to assess whether the intrinsic advantage of ion implantation in terms of reproducibility and uniformity can be effectively utilized in the fabrication of highly linear transistors.

This type of assessment will be carried out by comparing the relative merits of an idealized epitaxial profile with abrupt doping transition towards the substrate and the profile resulting from a 500 keV Se implant compensated at the surface by a shallow 40 keV Be implant. These profiles are shown in Fig. 2-11 along with a conventional flat doping profile, which will serve as a reference for the predicted performance. The ion implanted profile and the non-flat epitaxial profile of Fig. 2-11 represents a class of profile which should exhibit improved linearity. They do not represent the optimized condition, but rather are typical of what profile changes will give much better linearity.

The modified Pucel model was used to derive the G_m and G_d polynomial coefficients for these three profiles. The results are shown in Tables 2-1 and 2-2. It is important to note that the magnitude of the fifth-order coefficients is least for the ion implanted profile promising a better high power IMD performance. It is also noteworthy that in the case of transconductance, G_{m5} is larger than the G_{m3} coefficient for the flat profile device.

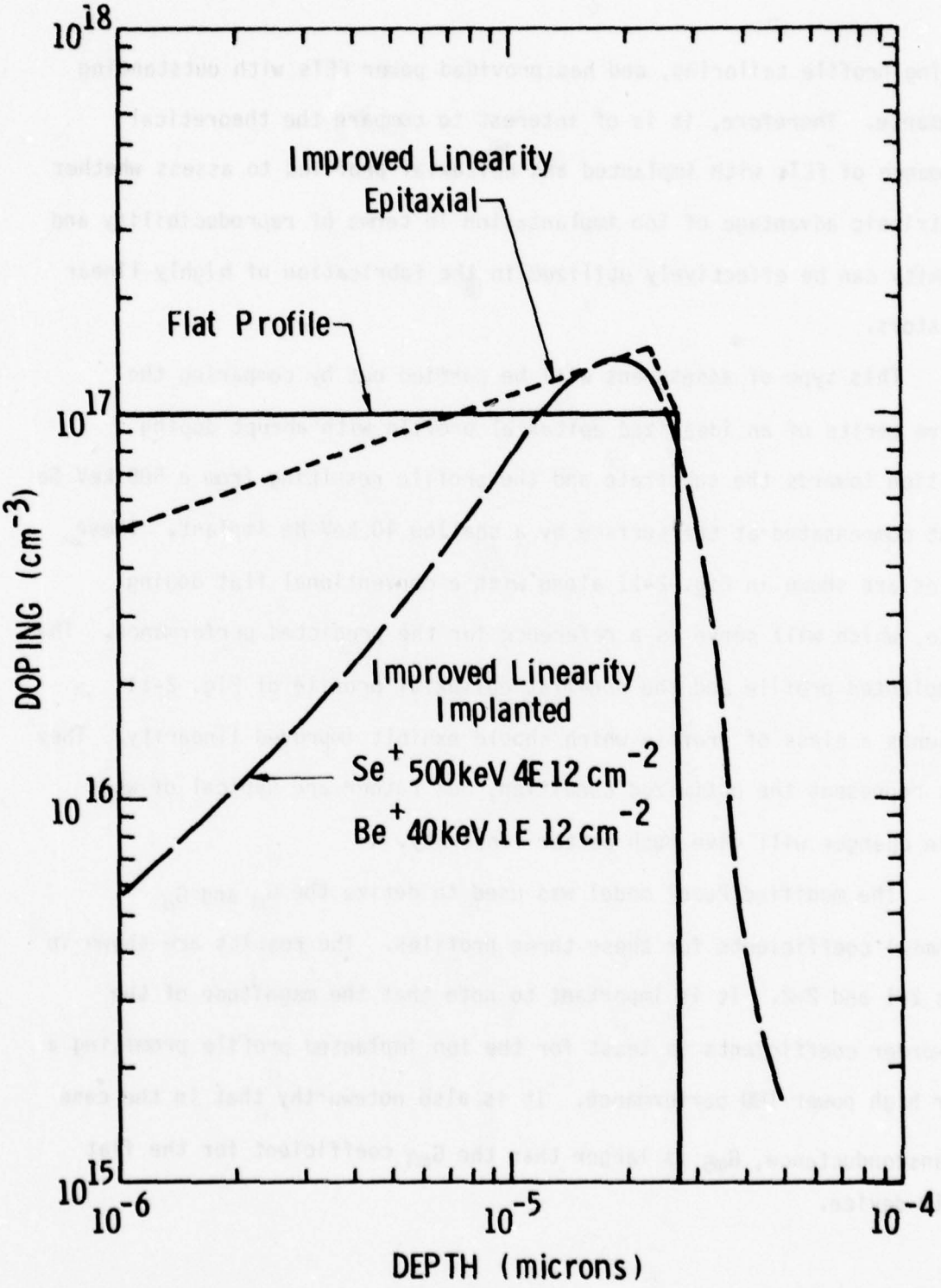

Fig. 2-11 Implanted and epitaxial doping profiles used in calculating the IMD characteristics of GaAs FETs.

TABLE 2-1

POLYNOMIAL COEFFICIENTS OF TRANSCONDUCTANCE

Coefficient	Flat Epi	Optimized Epi	Ion Implant Se + Be
G_{m1}	.035	.0355	.031
G_{m2}	.0058	.004	.0033
G_{m3}	-.00045	-.0007	.00075
G_{m4}	.00033	.00058	-.000054
G_{m5}	.00146	.0009	-.0002
G_{m6}	.00005	-.0001	.000042
G_{m7}	-.0002	-.0001	.0000448
G_{m8}	.000005	.000015	-.0000047

TABLE 2-2

POLYNOMIAL COEFFICIENTS OF OUTPUT CONDUCTANCE

Coefficient	Flat Epi	Optimized Epi	Ion Implant Si + Be
G_{d1}	1.64 E-4	1.99 E-4	4.28 E-4
G_{d2}	-3.07 E-5	-4.19 E-5	-4.90 E-5
G_{d3}	1.134 E-5	5.18 E-6	-2.23 E-6
G_{d4}	-1.37 E-6	7.62 E-7	1.23 E-7
G_{d5}	-3.92 E-7	-2.25 E-7	1.26 E-7
G_{d6}	5.80 E-8	-8.47 E-9	-2.02 E-8
G_{d7}	6.20 E-9	5.4 E-9	2.00 E-9
G_{d8}	-8.21 E-10	-3.41 E-10	-1.08 E-10

The corresponding coefficients for the gate-source capacitance are given in Table 2-3 for the flat profile and the optimized Se + Be implant. The magnitude of the coefficients reflects the smaller variation in this capacitance vs gate voltage for the implanted profile, which should reduce gain expansion effects and minimize IMD contributions from this source.

The derived coefficients will be used in the next section to calculate the IMD performance and gain saturation behavior resulting from the three profiles in Fig. 2-11.

Table 2-3

POLYNOMIAL COEFFICIENTS OF GATE-SOURCE CAPACITANCE

Coefficient	Flat Epi	Ion Implant Se + Be
C_{g1}	.2786	.2482
C_{g2}	.0467	.0245
C_{g3}	.0127	.00029
C_{g4}	.0004	.0005
C_{g5}	-.0016	-.0003
C_{g6}	.0025	.0002
C_{g7}	.0012	.00007
C_{g8}	-.0008	-.00004

2.3 Intermodulation Distortion

The calculated IMD is based upon the normal two-tone-of-equal-power test. The procedure is straightforward but some very important points must be

emphasized. Only third-order products have been calculated. Normally, it is assumed that the third-order coefficient (G_{m3} for instance) is much larger than the fifth or seventh order coefficients (G_{m5}, G_{m7}). From Table 2-1 this is evidently not so. From an expansion of the higher order terms in Eqs.(1) or (3), it is seen that fifth-order coefficients do contribute substantially to third-order IMD products. In fact, for moderate to high signal levels the transconductance contributes mainly from its fifth (G_{m5}) coefficient term. This is seen from Table 2-4 and 2-5 where the contributions to power saturation and to each IMD product from the various coefficients are tabulated. This observation provides an explanation of the phenomena of "non well behaved IMD products" described by Strid and Duder.[2]

The second point to be made is that in the low power signal region, the IMD contributions of the drain conductance G_d dominate, and, as the signal level rises, the G_m contributions to IMD products become larger. The

Table 2-4

The ω_1 components resulting from driving a nonlinear conductance
$G = G_1 + G_2V + G_3 V^2 + G_4 V^3$.....with a two-tone signal
$V = A \sin(\omega_1 t) + B \sin(\omega_2 t)$

Source	Component	Component if B=0
G_1V	A	A
G_3V^3	$.75A^3 + 1.5A^2B$	$.75A^3$
G_5V^5	$.625A^5 + 3.75A^3B^2 + 1.875AB^4$	$.625A^5$

TABLE 2.5

TWO-TONE TEST INTERMODULATION PRODUCTS

$V_1 = A \cos \omega_1 t + B \cos \omega_2 t$

	Third	Fifth	Seventh	Ninth
IMD Source	$2f_1 - 2f_2$	$3f_1 - 2f_2$	$4f_1 - 3f_2$	$4f_1 - 4f_2$
$(G_3x)\ V^3$	$.75A^2B$			
$(G_5x)\ V^5$	$1.25A^4B$	$.625A^3B^2$		
	$1.875A^2B^3$			
$(G_7x)\ V^7$	$1.64A^6B$	$1.64A^5B^2$	$.547A^4B^3$	
	$6.56A^4B^3$	$2.187A^3B^4$		
	$3.28A^2B^5$			
$(G_9x)\ V^9$	$1.97A^8B$	$2.95A^7B^2$	$1.969A^6B^3$	$.49A^5B^4$
	$14.76A^6B^3$	$9.84A^5B^4$	$2.46A^4B^5$	
	$19.687A^4B^5$	$4.92A^3B^6$		
	$4.92A^2B^7$			

i.e., for $G_3 \neq 0$ $G_5 \neq 0$ $G_{n>5} = 0$

$$I_{2f_1 - f_2} = .75\ G_{m3}A^2B + 1.25\ G_{m5}A^4B + 1.875\ G_{m5}A^2B^3$$

nonlinearities due to the transconductance and the output conductance can be expected to be partially correlated as a result of the coherence between the gate and the drain voltages. This correlation can give rise to a cancellation effect in the IMD products. This type of behavior is commonly observed as illustrated in Fig. 2-1 and by the results in Sec. 4.3.

The sign of the fifth-order coefficient relative to the third-order coefficient may be quite important in determining the low signal level IMD products. In fact, cancellation effects can occur in third-order IMD products

from the drain (or gate) alone due to sign differences of the different coefficients.

2.3.1 Profile Effects on IMD

The equivalant circuit in Fig. 2-2 has been used in conjunction with the information in Tables 2-1 to 2-5 to calculate the gain saturation and the third order intermodulation products of the three profiles shown in Fig. 2-11. The results are given in Fig. 2-12.

It is observed that the gains at small signal levels of both epitaxial devices are about 1 dB greater than the corresponding gain of the implanted transistor. This calculation is for a 10 GHz test where the signals (two tones) are separated by only a few MHz. The gain of the ion implanted device is less but saturates more slowly at high output power levels.

The IMD products display three distinct regions. At very low signal level, the third-order products rise 3 dB for a 1 dB increase in signal level. This behavior is explained by the dominant role of G_{d3} in this range. Then comes the intermediate signal level region where the cancellation effects are generally seen. Sometimes quite sharp dips are seen in this region and a representation of this effect has been depicted in Fig. 2-12 by a dotted line. In the large signal region, generally the contribution from the transconductance G_m dominates and the rate of rise of the IMD product is greater than third-order. This strong increase is caused by the large contribution from G_{m5} which may equal or exceed G_{m3}. Ion implantation displays a considerable advantage in this area because G_{m5} is much less than G_{m3} for this case and is lower than equivalent values for the other

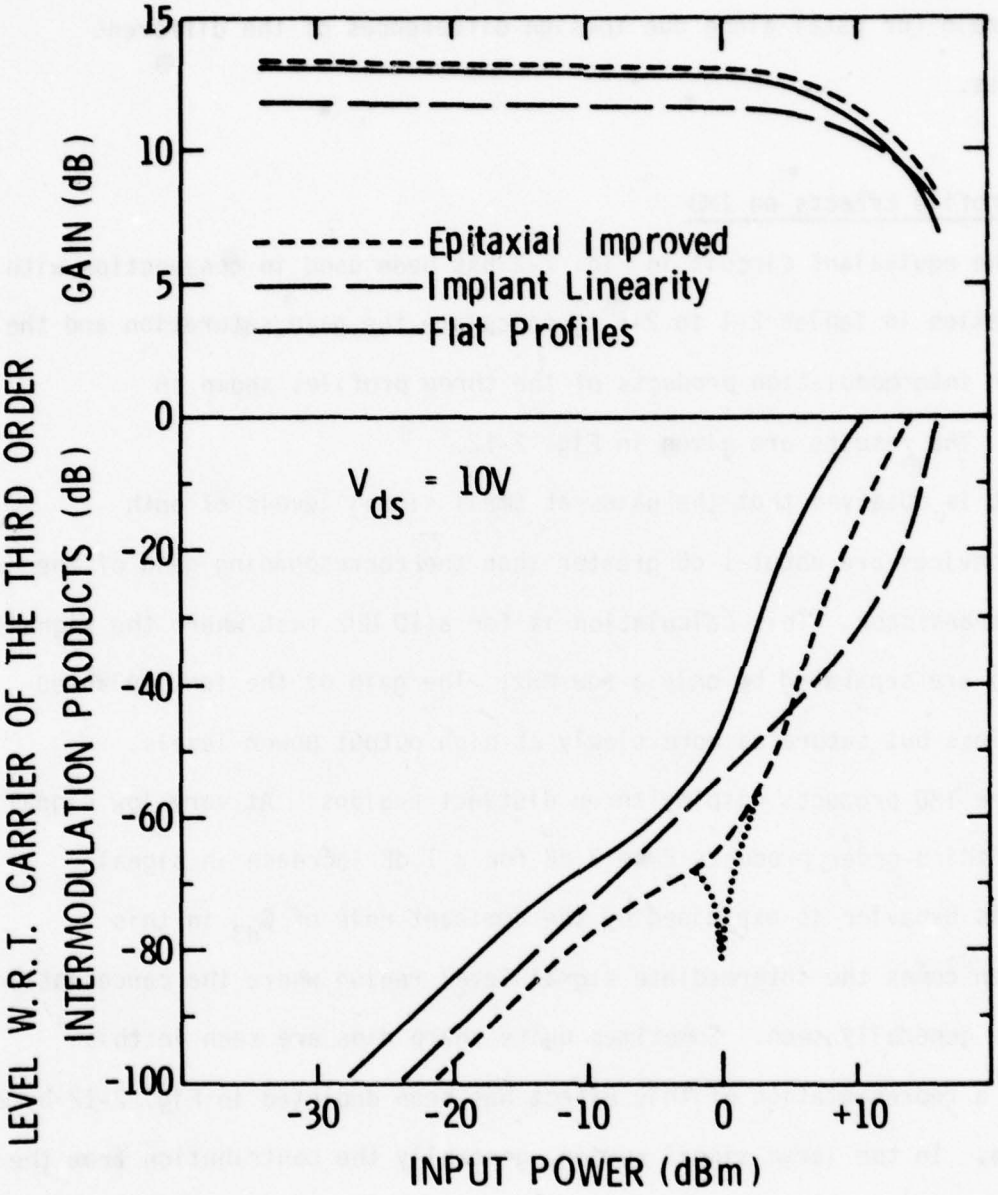

Fig. 2-12 Calculated gain and third order intermodulation products vs input power using the active layer profiles in Fig. 2-11.

profiles. This results in the IMD product for the ion implanted FET continuing to have lower IMD products to higher power levels before complete saturation occurs.

At the point of saturation where output power is considerable and gain is falling to low values, the IMD products of the simple model become inaccurate. The rate of rise of the IMD products should fall off as illustrated in Fig. 2-1 rather than continuing to rise at the higher rate shown in Fig. 2-11. The reason for this discrepancy is that the assumption of small IMD voltages becomes inaccurate and the total power is rapidly diverted into an increasing number of unwanted IMD products other than the third order products. This area of the IMD vs input power level is tractable to computation using methods which (a) account for many frequencies of non-negligible voltage level, (b) account for the total power distribution and (c) extend the power series representation for the equivalent circuit elements to a sufficiently high order.

A second example of the excellent linearity available from implanted profiles is given in Fig. 2-13. This calculation assumed an optimized dual dose Si implant, which qualitatively is similar to the Si + Se profile in Fig. 2-9. A comparison with the results in Fig. 2-12 reveals that the available gain and the saturated power output is comparable to the optimized epitaxial profile, while the third order intermodulation product is somewhat lower for the implanted structure at high power levels.

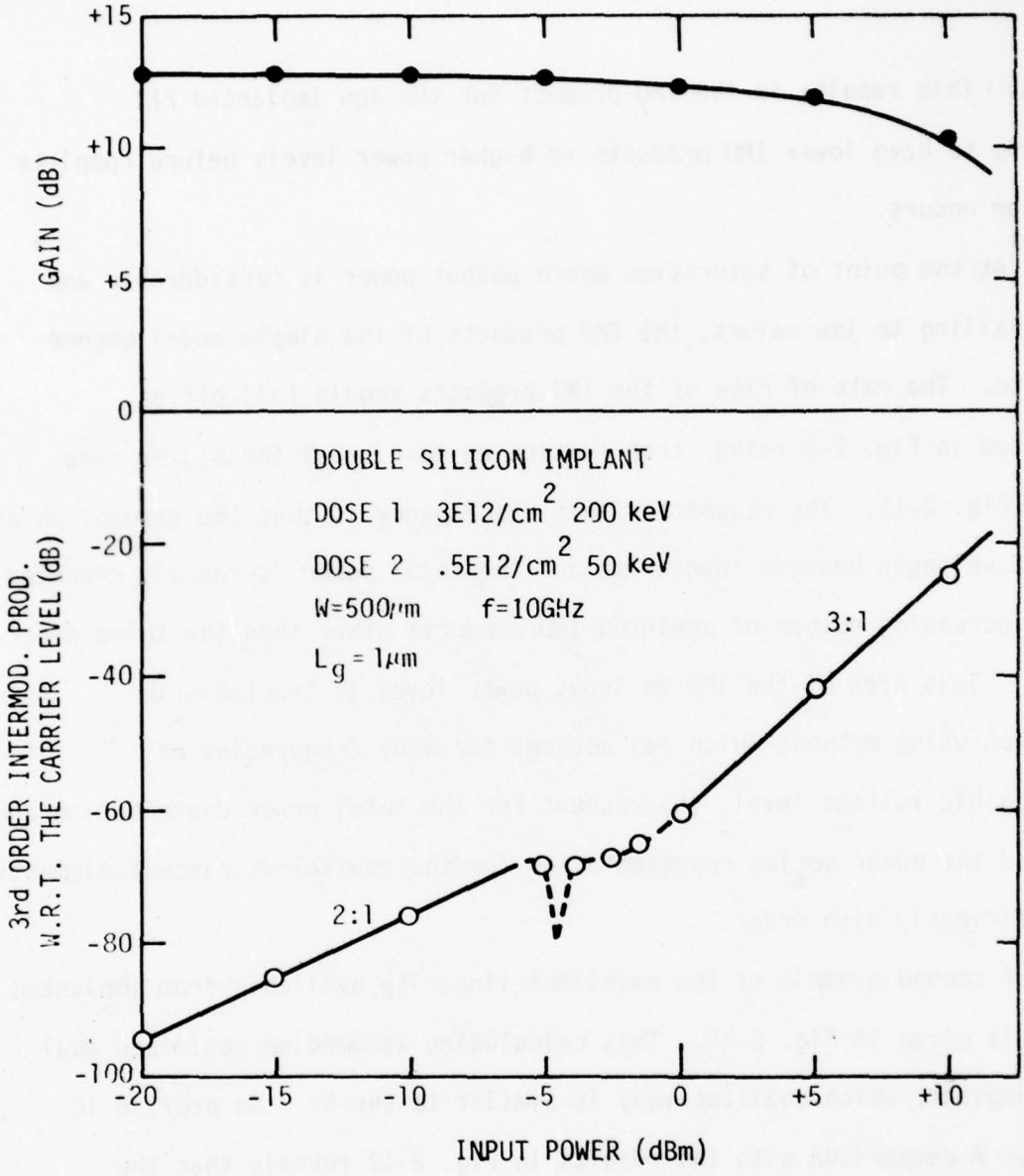

Fig. 2-13 Calculated gain and third order intermodulation product vs input power for Si implanted GaAs FET.

2.3.2 Bias Dependence

The dependence of IMD on drain bias level has been calculated for the implanted profile in Fig. 2-11. The principal result of a change of drain bias is a general reduction of the G_d coefficients with a rise of the bias voltage. This effect is illustrated by the results in Table 2-6, which lists the expansion coefficients of G_d for drain bias voltages of 6 and 10 V. The resulting IMD products have been calculated and are shown in Fig. 2-14. The IMD products rise for a drop in drain bias, both at the low power end and at

TABLE 2-6

Polynomial Coefficients of Drain Conductance for Different Drain Bias Conditions

Coefficient	V_{DS} = 6V	V_{DS} = 10V
G_{d1}	3.32 E-4	4.28 E-4
G_{d2}	5.04 E-4	-4.90 E-5
G_{d3}	2.10 E-3	-2.23 E-6
G_{d4}	-6.47 E-4	1.23 E-7
G_{d5}	-5.12 E-4	1.26 E-7
G_{d6}	1.29 E-4	-2.02 E-8
G_{d7}	3.10 E-5	-2.00 E-9
G_{d8}	-7.00 E-6	-1.08 E-10

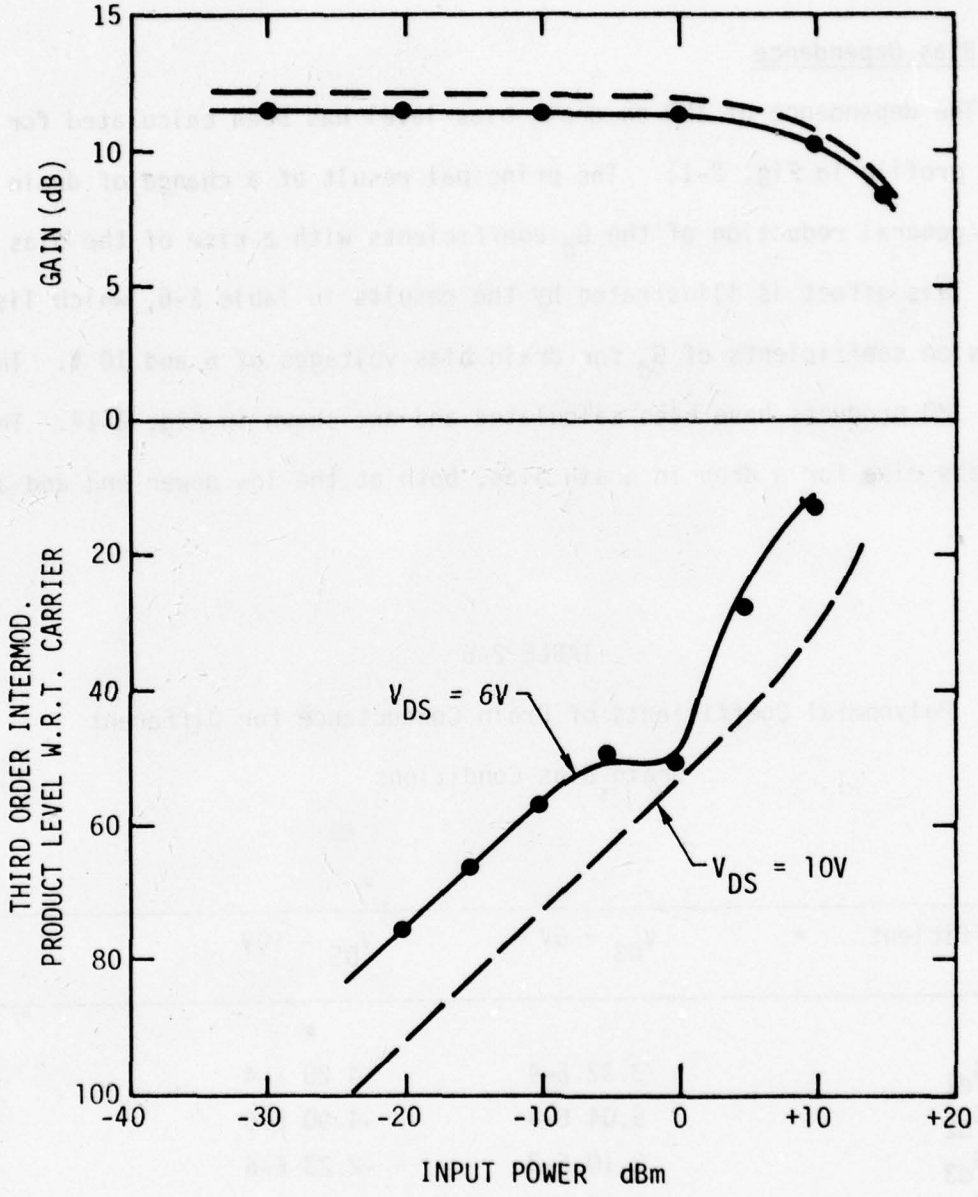

Fig. 2-14 Calculated gain and third order intermodulation product vs input power for implanted GaAs FET with the drain voltage as a parameter.

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moderately high input power levels. A more pronounced cancellation notch is noted at the lower drain bias because of the increase in the IMD products due to G_d. It is interesting to note that these results also correspond quite closely to experimentally observed results in Sec. 4.3.

3.0 DEVICE FABRICATION

The primary goal of this development program was to realize highly linear GaAs power FETs by tailoring of ion implanted profiles to optimize the doping in the active layer. Therefore, the major development effort in the area of device fabrication was devoted to preparation of suitable active layers. Several different combinations of implant conditions and species were carried out towards this end. The resulting profiles will be presented in this section.

Standard processing techniques were used in completing the fabrication of the transistors and will be briefly reviewed for completeness.

3.1 Ion Implantation Profiles

The theoretical calculation in Sec. 2 indicated that Si, Se and surface compensated Se + Be implants all can provide suitable layers for power FETs with good linearity. All these possibilities were tried in this program.

Early efforts were devoted to establishing the characteristics of Si implants due to the favorable skewness of the expected profile. The result of a 200 keV implant with a dose of $4 \times 10^{12} cm^{-2}$ is shown in Fig. 3-1. The measured profile agrees well with the range parameters and expected outdiffusion for Si implants. The doping is characterized by a positive slope at the surface, a deep buried peak and a steep transition region towards the substrate. This type of retrograde profile is close to optimum for realizing low IMD products as discussed in Sec. 2.3. Problems with inconsistent

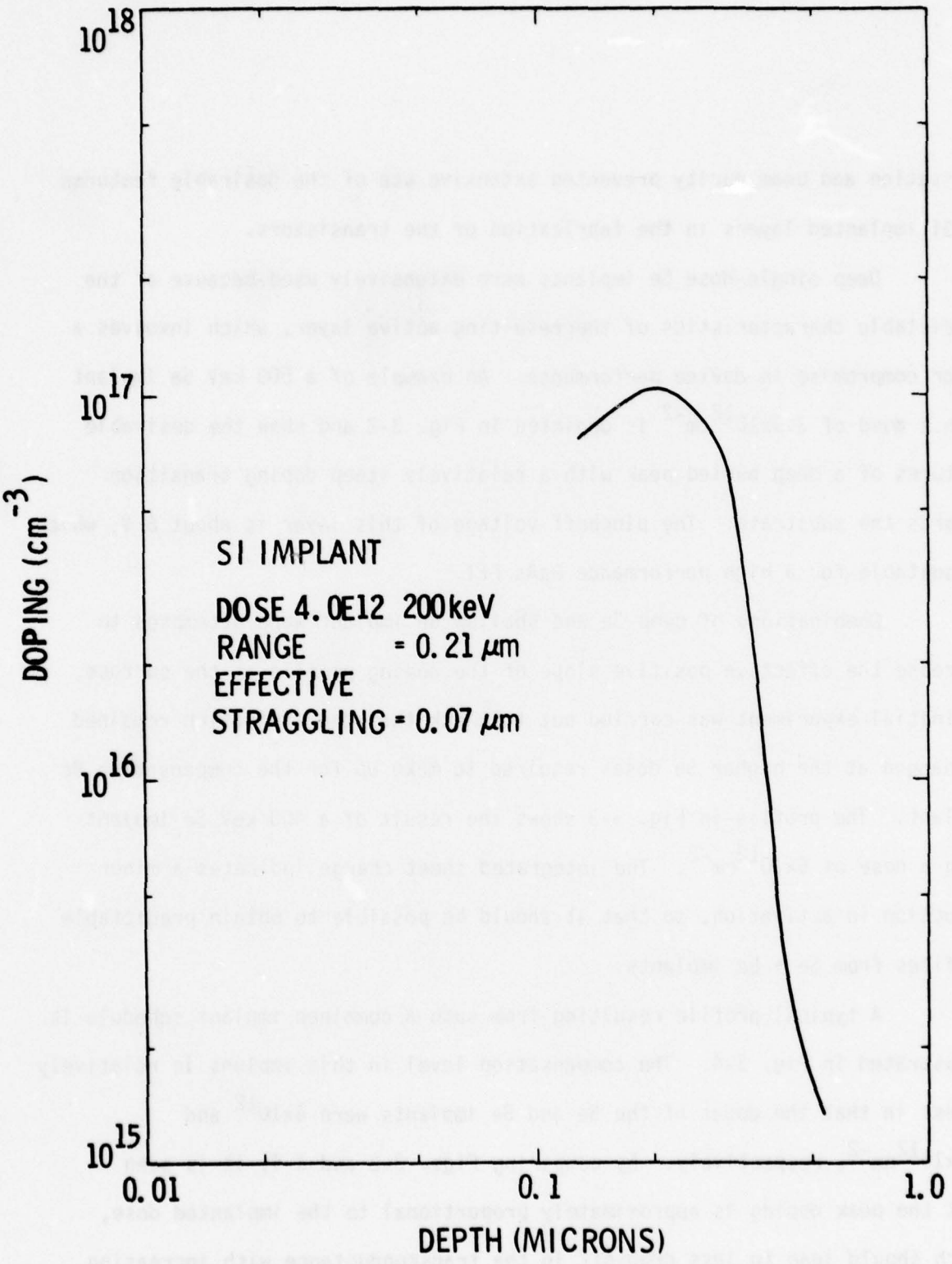

Fig. 3-1 Measured doping profile for 200 keV Si implant with a dose of $4 \times 10^{12} cm^{-2}$.

activation and beam purity prevented extensive use of the desirable features of Si implanted layers in the fabrication of the transistors.

Deep single-dose Se implants were extensively used because of the predictable characteristics of the resulting active layer, which involves a minor compromise in device performance. An example of a 500 keV Se implant with a dose of $3.5 \times 10^{12} cm^{-2}$ is depicted in Fig. 3-2 and show the desirable features of a deep buried peak with a relatively steep doping transition towards the substrate. The pinchoff voltage of this layer is about 6 V, which is suitable for a high performance GaAs FET.

Combinations of deep Se and shallow Be implant were attempted to increase the effective positive slope of the doping profile at the surface. An initial experiment was carried out to check that the activation remained unchanged at the higher Se doses required to make up for the compensating Be implant. The profile in Fig. 3-3 shows the result of a 400 keV Se implant with a dose of $6 \times 10^{12} cm^{-2}$. The integrated sheet charge indicates a minor reduction in activation, so that it should be possible to obtain predictable profiles from Se + Be implants.

A typical profile resulting from such a combined implant schedule is illustrated in Fig. 3-4. The compensation level in this implant is relatively modest in that the doses of the Se and Be implants were 4×10^{12} and $0.5 \times 10^{12} cm^{-2}$, respectively. By comparing Figs. 3-2 and 3-4, it is seen that the peak doping is approximately proportional to the implanted dose, which should lead to less drop-off in the transconductance with increasing gate bias and thus better linearity for the combined Se + Be implant.

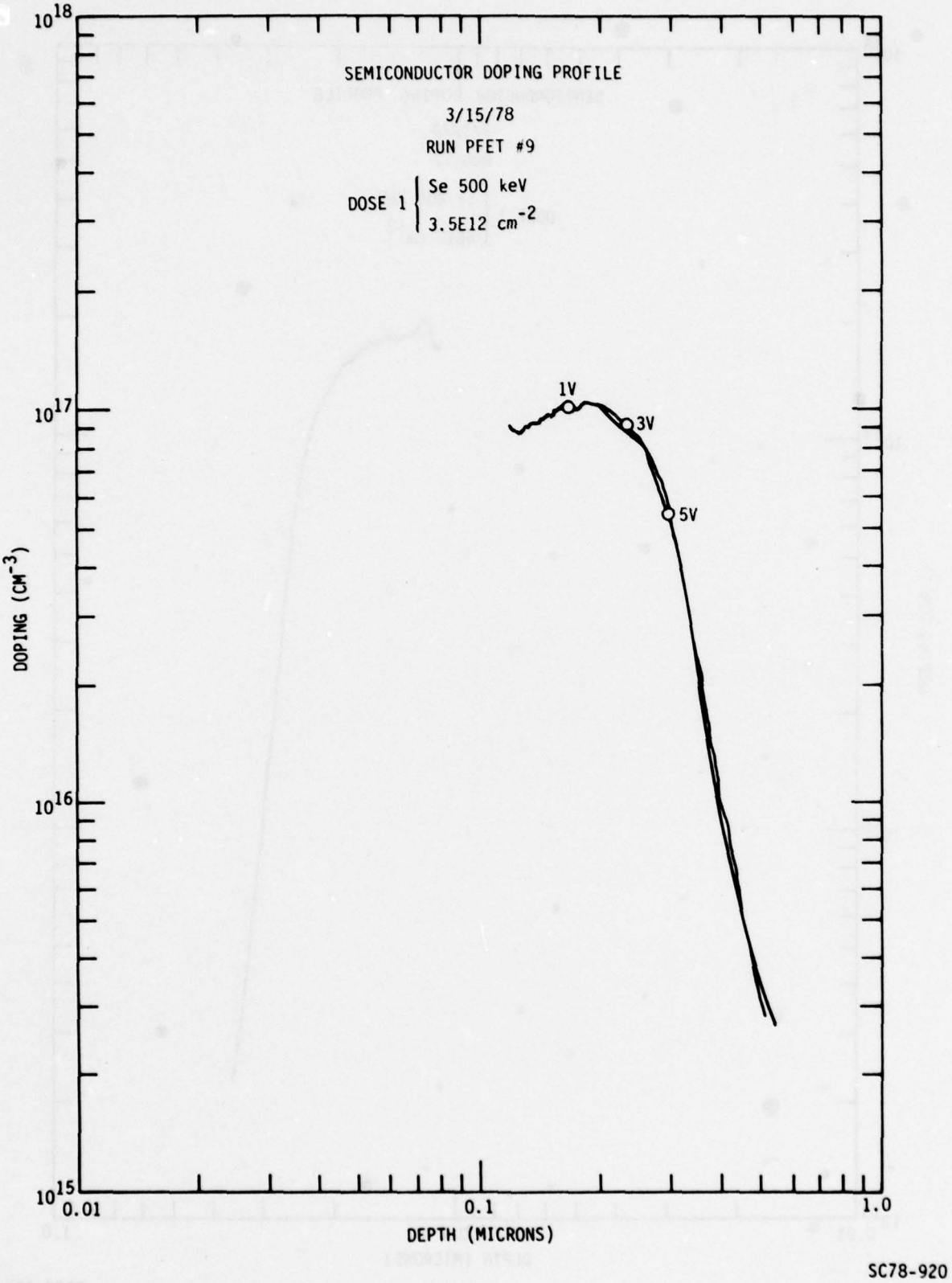

Fig. 3-2 Measured doping profile for 500 keV Se implant with a dose of $3.5 \times 10^{12} cm^{-2}$.

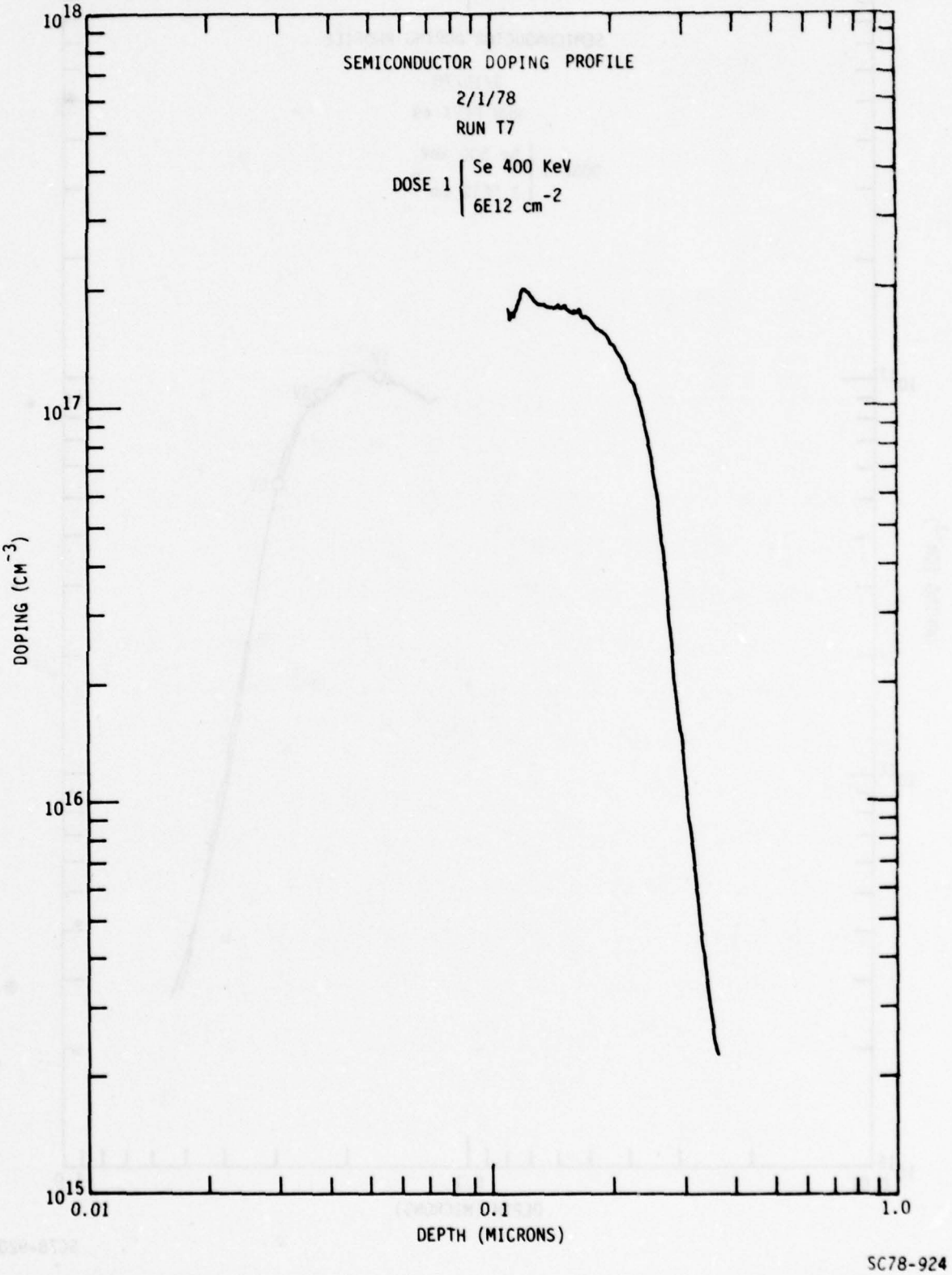

Fig. 3-3 Measured doping profile for 400 keV Se implant with a dose of $6 \times 10^{12} cm^{-2}$.

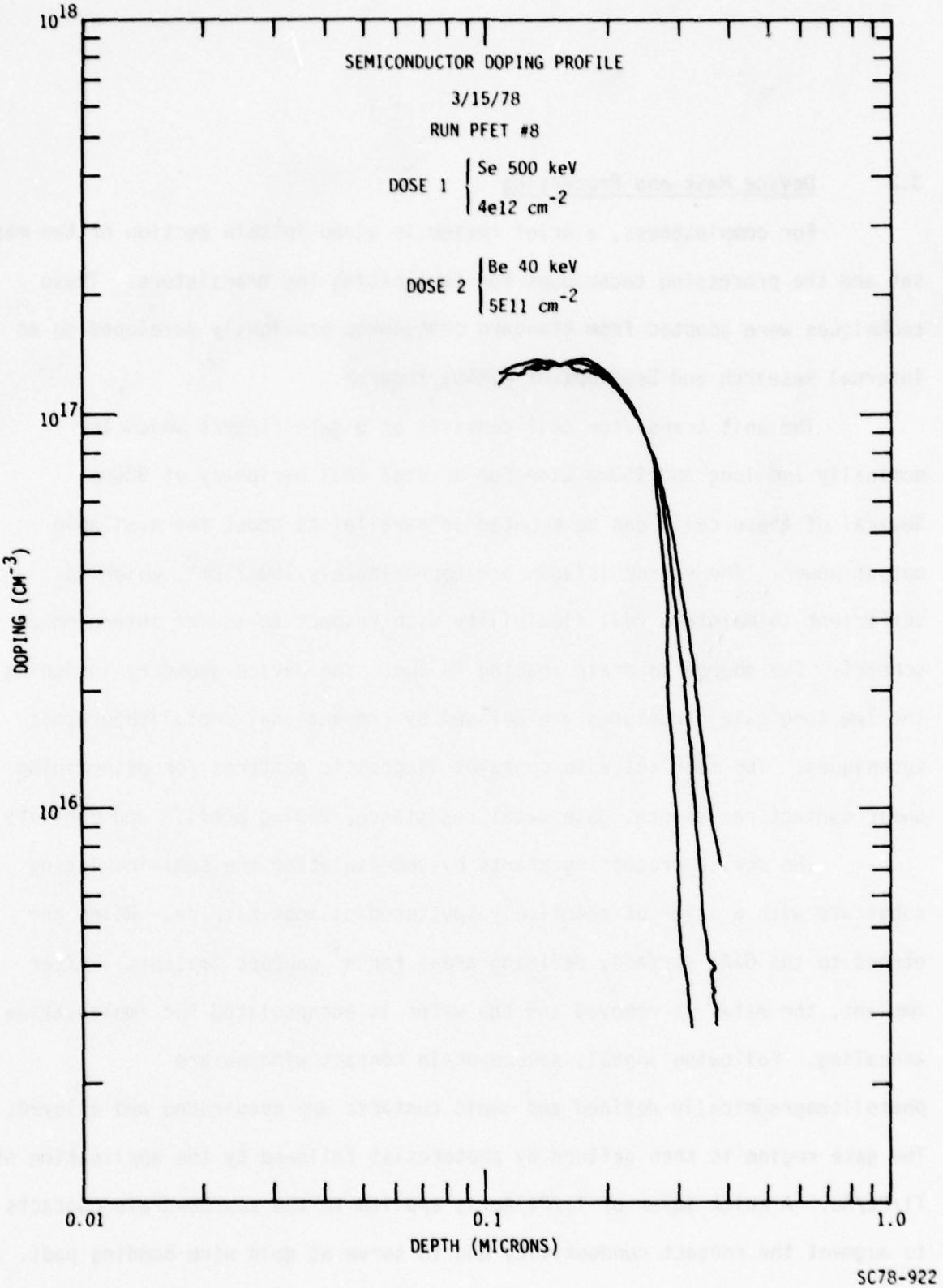

Fig. 3-4 Measured doping profile for combined 500 keV Se ($4x10^{12}cm^{-2}$) and 40 keV Be ($0.5x10^{12}cm^{-2}$) implants.

3.2 Device Mask and Processing

For completeness, a brief review is given in this section of the mask set and the processing techniques for fabricating the transistors. These techniques were adopted from standard procedures previously developed on an Internal Research and Development (IR&D) Program.

The unit transistor cell consists of 6 gate fingers which are nominally 1μm long and 150μm wide for a total cell periphery of 900μm. Several of these cells can be mounted in parallel to boost the available output power. The source islands are approximately $150x75\mu m^2$, which is sufficient to maintain full flexibility with respect to source interconnect schemes. The source to drain spacing is 5μm. The device geometry including the 1μm long gate structures are defined by conventional photolithographic techniques. The mask set also contains diagnostic patterns for determining ohmic contact resistance, gate metal resistance, doping profile and mobility.

The device processing starts by encapsulating the semi-insulating substrate with a layer of reactively sputtered silicon nitride. Holes are etched to the GaAs surface, defining areas for n^+ contact implants. After implant, the metal is removed and the wafer is encapsulated for implantation annealing. Following anneal, source-drain contact windows are photolithographically defined and ohmic contacts are evaporated and alloyed. The gate region is then defined by photoresist followed by the application of Ti/Pt/Au. A thick layer of Ti/Pt/Au is applied to the source-drain contacts to augment the contact conductivity and to serve as gold wire bonding pads. The finished transistors are mounted on the central ridge of a power FET package featuring a heavy gold plated OFHC base and input-output transformers on alumina substrates for partial matching of the transistor impedance.

4.0 DEVICE CHARACTERIZATON

The evaluation of the fabricated power FETs has included diagnostic as well as performance measurements. The diagnostic information has primarily come from measuring the I-V characteristics and small-signal S-parameters. Elements of an equivalent circuit model for the basic chip has been established based on these measurements. Extensive investigations of intermodulation products vs input power level have been carried out to address the main objective of this development, which was to realize highly linear RF behavior by tailoring the doping profile of the active layer. In addition, the power generating capability of the transistors were assessed by tuning for maximum output at large-signal drive levels.

A reference for the observed characteristics was obtained by performing similar measurements on power FETs with a flat doping profile. These transistors were fabricated from VPE material on an IR&D program. The measurement results and the comparison of the ion implanted and VPE FETs are presented in this section.

4.1 DC Characteristics

The merits of using selective implants for realizing highly doped n^+ source and drain contact regions were explored on this program, by fabricating FETs with and without the enhanced contact doping on the same wafer. As expected, a significant reduction of the specific contact resistivity was found by employing the additional n^+ implant. A value of $1x10^{-6}$ ohm-cm^2 was estimated in several cases for the specific resistance

of the n^+ implanted areas, compared to a resistivity of $4x10^{-6}$ohm-cm^2 in the absence of the added implant. However, in some cases, an abnormally high resistivity was found for the highly doped contact regions indicating a greater sensitivity to the alloying of the ohmic contacts. This problem is under further study on an IR&D program. The intermodulation products are dependent upon the ohmic contacts inasmuch as the device current saturation characteristics is. It is felt that lower gain and higher intermodulations result when ohmic contacts become more resistant.

The transistors must be able to sustain high drain voltage levels in order to maximize the RF output power. Therefore, it is vitally important to realize high breakdown voltages for the transistor. Early lots fabricated on this development program broke down at a drain voltage of about 16V, while the later lots can sustain about 25V dc drain bias under pinchoff conditions. As a result, drain bias levels to 10 to 15V have been used routinely in the RF evaluation of the latter transistors. These voltages are sufficient for maximizing the output power. The electrical characteristics of the gate Schottky barrier are of prime importance with respect to attaining reliable device operation with adequate margin for RF transients. The ruggedness of the Ti/Pt/Au metalization has been verified by measuring the I-V characteristic of the gates with the source and the drain contacts grounded. Reverse voltages in excess of 10V can be sustained with less than 10nA leakage current, while greater than 100mA forward current can be applied without affecting the quality of the gate Schottky contact.

Typical I-V characteristics of an ion implanted single cell transistor are shown in Fig. 4-1. The saturation voltage for this transistor is about 2.5V. The saturated drain current is 160mA, which is

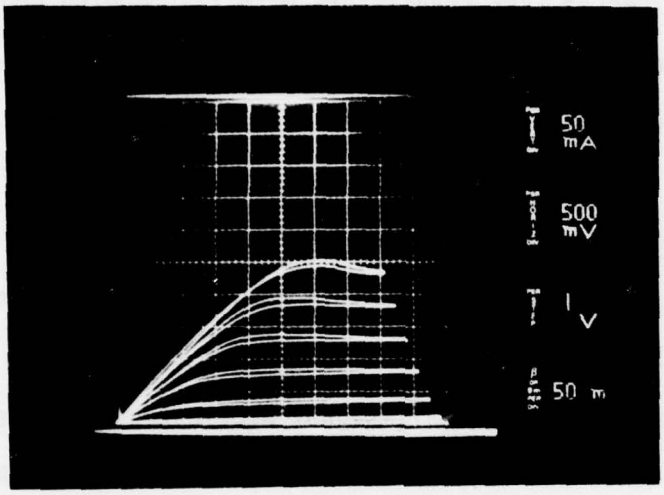

Fig. 4-1 Measured I-V characteristics of Se + Be implanted GaAs FET.

somewhat lower than desired. The transconductance is about 50mS and remains fairly constant down to pinchoff, which indicates that the profile is close to optimum. As expected, VPE transistors with flat doping profiles were found to display considerably larger variation in the transconductance as a function of gate voltage.

4.2 S-Parameters

Some transistors were mounted in a 70 mil metal-ceramic package to facilitate broad band S-parameter measurements. This package is normally used for low-noise devices in small-signal applications and is not suitable for power measurements due to poor thermal characteristics. An optimization routine has been used to match measured S-parameter data to an equivalent circuit for the transistor as shown in Fig. 4-2. The typical range of the input capacitance at 0.5 I_{DSS} is 0.8-1.0pF where the lower values correspond to transistors with a shallow compensating Be implant at the surface. The transconductance is typically 50mS in good agreement with observed dc characteristics. The relatively high source inductance of 0.1nH is caused by the limited bonding space in the small-signal package, which prevents the realization of a low-parasitic interconnect scheme between the source pads. The high common source inductance degrades the transfer characteristics S_{21} and S_{12} at higher frequencies.

This shortcoming is eliminated for transistors mounted on the power package. Typical results from these transistors biased at 0.5 I_{DSS} show that the magnitude os S_{21} drops from 2.4 at 4 GHz to 1.8 at 9 GHz, while S_{12} increases from 0.02 at 4 GHz to 0.045 at 9 GHz indicating excellent gain performance. This observation has been confirmed by measured small-signal gains in excess of 15 dB at 7 GHz and 11 dB at 10 GHz.

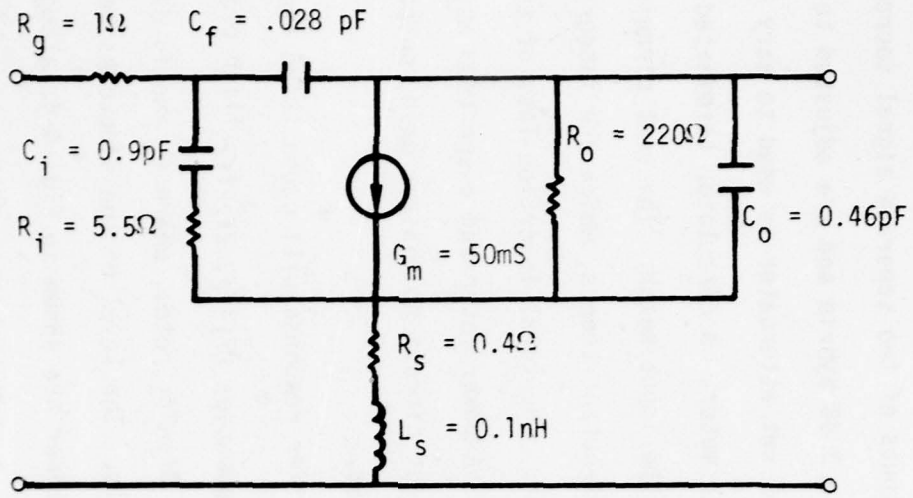

Fig. 4-2 Equivalent circuit of implanted GaAs power FET.

4.3 Intermodulation Measurements

The intermodulation distortion of the developed transistors has been measured by using the two-tone method. The layout of the experimental setup is shown in Fig. 4-3. The outputs of two separate signal sources offset by a few MHz are combined in a 3 dB hybrid and are adjusted to equal incident power to the FET. The level set attenuator is used to vary the RF input power, which is read by a power meter. A circulator terminated in a crystal detector is used to monitor the input match. The test circuit consists of coaxial double-slug input-output tuners, which are integrated with the heat sink for the transistor. The total insertion loss of the test circuit is less than 1 dB at 10 GHz. A power meter and a spectrum analyzer are connected to the output of the test circuit to monitor gain, output power and the intermodulation products.

Nonlinearities in the amplifier response will cause third order mixing products to appear at the frequencies $2f_1-f_2$, $2f_2-f_1$; fifth order products at the frequencies $3f_1-2f_2$, $3f_2-2f_1$, etc., where f_1 and f_2 denote the frequencies of the primary signals. The level of the sidetones measured at 10 GHz as functions of the input power are shown in Fig. 4-4, along with the gain saturation curve for a Se implanted transistor (A1D1, $3\times10^{12}cm^{-2}$ Se ions at 400 keV) operated at a drain voltage of 10V. The tuning conditions of this transistor show strong correlation effects as evidenced by the scalloping of the sidetones. Contrasting results are shown in Fig. 4-5 for another transistor (A3D2 $3\times10^{12}cm^{-2}$ at 400 keV) tuned to a linear gain of 8 dB compared to 11 dB in the previous case. This difference is thought to be due to ohmic contacts in the case of wafer A3 that do not come up to normal standards of high conductivity and therefore distort the I-V characteristic to lead to situations where the "drain" side distortion is

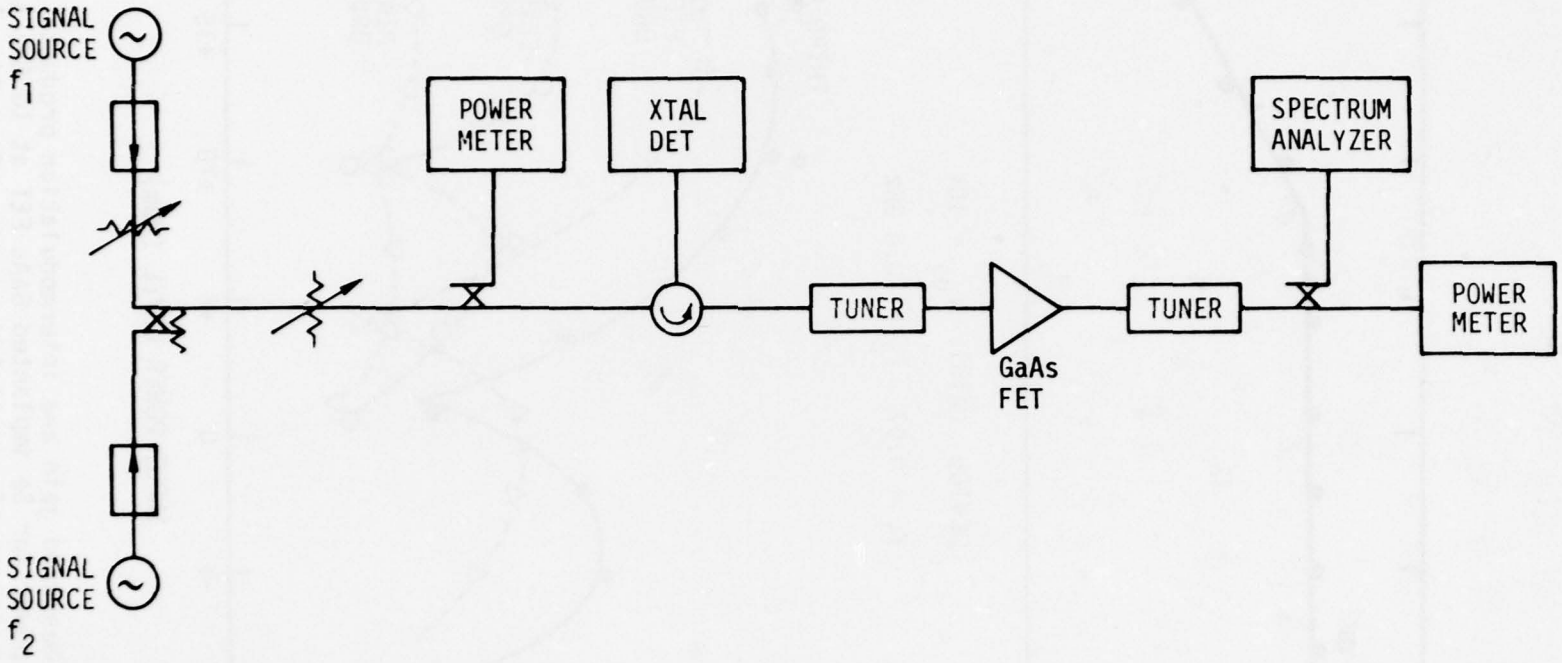

Fig. 4-3 Test set for measuring gain, power and intermodulation products of GaAs FET.

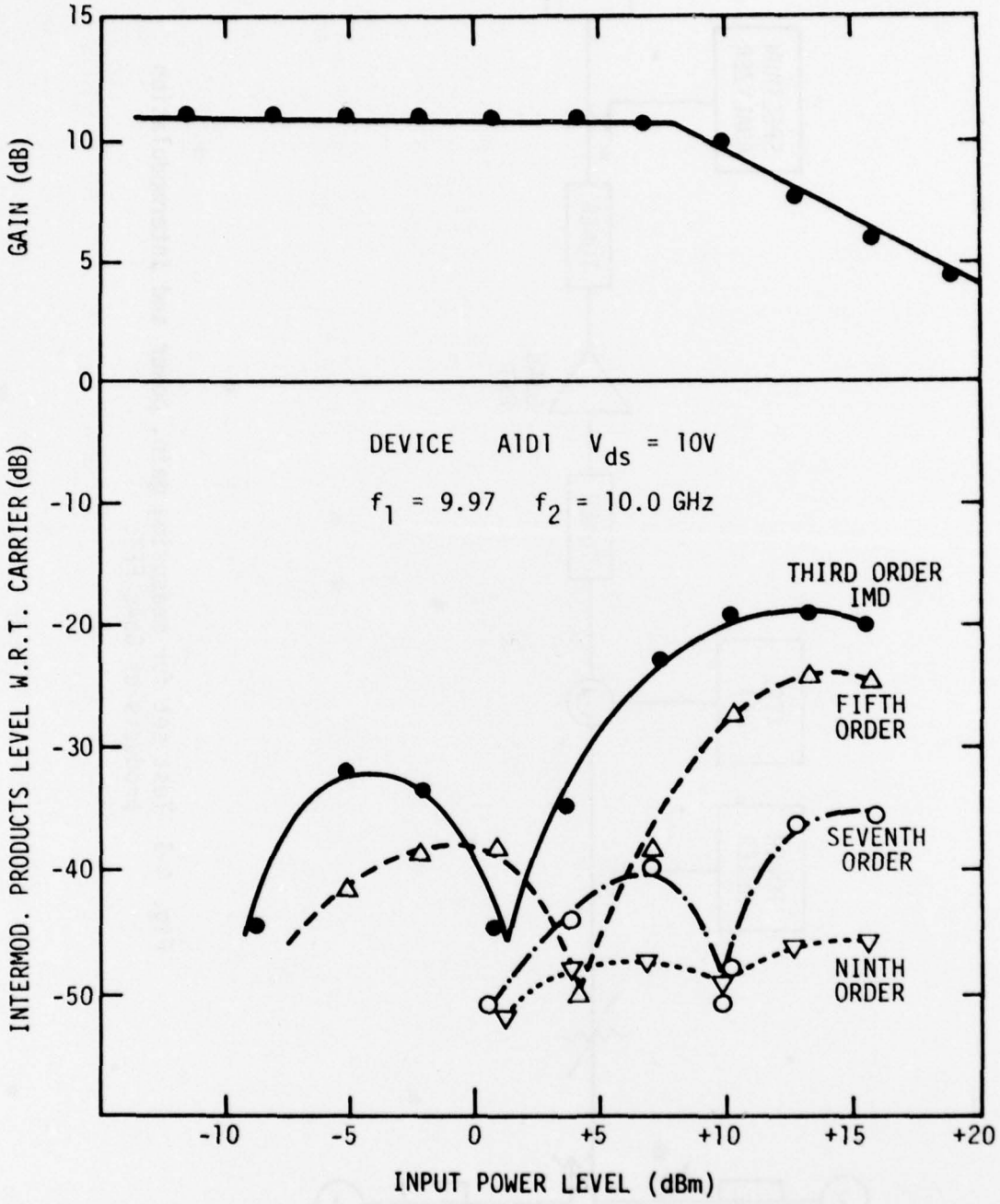

Fig. 4-4 Measured gain and intermodulation products vs input power for Se implanted GaAs FET at 10 GHz showing evidence of correlated sources of nonlinearity.....

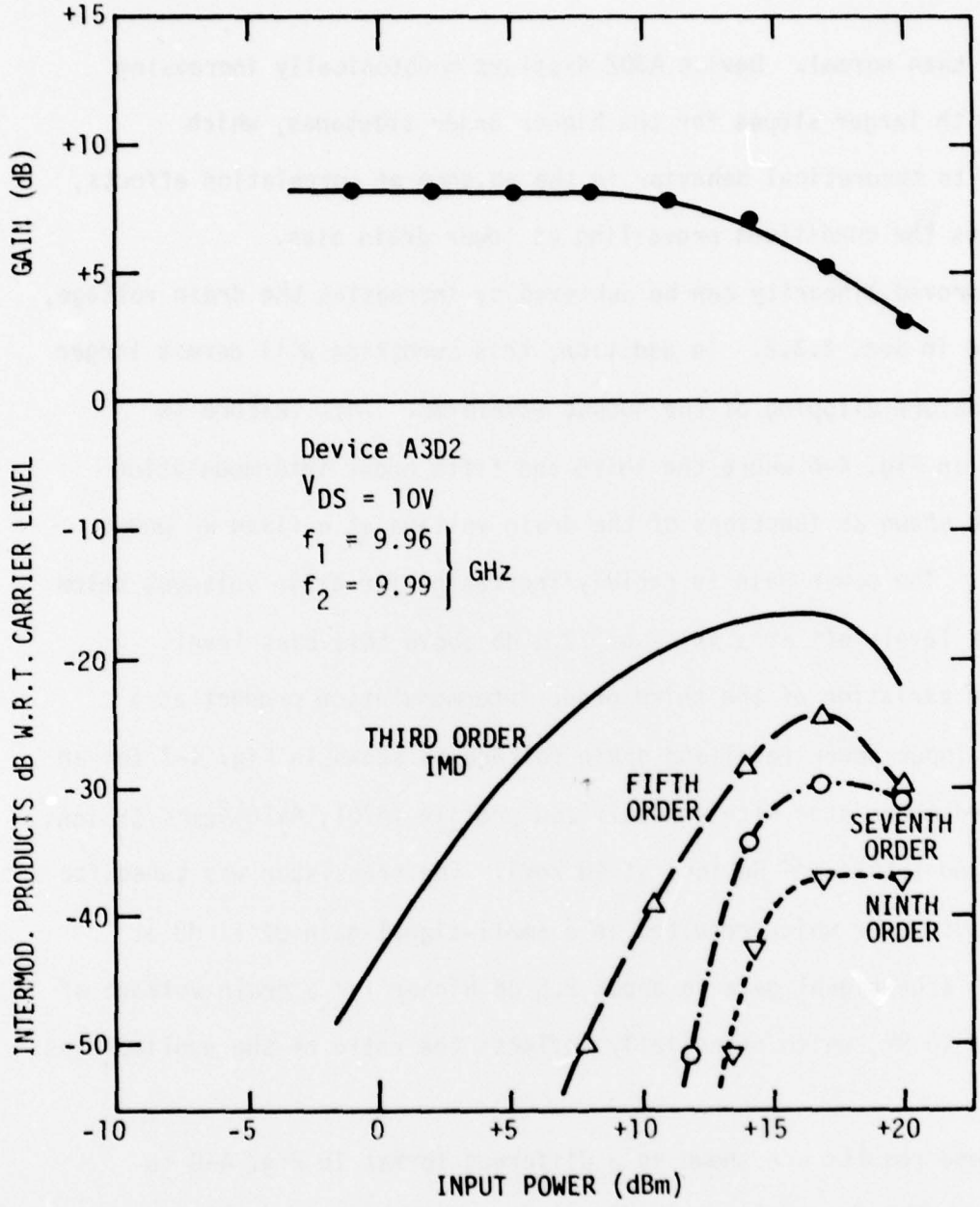

Fig. 4-5 Measured gain and intermodulation products vs input power for Se implanted GaAs FET at 10 GHz with minimal correlation between the sources of nonlinearity.

much higher than normal. Device A3D2 displays monotonically increasing sidetones with larger slopes for the higher order sidetones, which corresponds to theoretical behavior in the absence of correlation effects, and simulates the conditions prevailing at lower drain bias.

Improved linearity can be achieved by increasing the drain voltage, as discussed in Sec. 2.3.2. In addition, this condition will permit larger RF signals before clipping of the output waveforms. This feature is illustrated in Fig. 4-6 where the third and fifth order intermodulation products are shown as functions of the drain voltage at a fixed RF power input level. The power gain is rapidly increasing for drain voltages below 8V, while it levels off at a value of 12.5 dB above this bias level.

The variation of the third order intermodulation product as a function of input power level and drain voltage is shown in Fig. 4-7 for an ion implanted transistor with an optimized profile (A7D1, $4 \times 10^{12} cm^{-2}$ Se ions at 500 keV and $1 \times 10^{12} cm^{-2}$ Be ions at 40 keV). The transistor was tuned for optimum output power which resulted in a small-signal gain of 11 dB at 8 GHz. The large-signal gain is about 2.5 dB higher for a drain voltage of 14V compared to 8V, which essentially reflects the ratio of the applied bias powers.

These results are shown in a different format in Fig. 4-8 to illustrate the third order intercept point as a function of drain voltage. The lower lines with steep slopes represent the third order intermodulation products, while the upper curves give the output power. The intercept point for a drain bias of 8V is 33 dBm compared to 37 dBm for a drain bias of 14V.

The maximum small-signal gains of the power transistors are substantially higher than the corresponding linear gains when the FETs are tuned for maximum output power. This observation reflects the fact that the

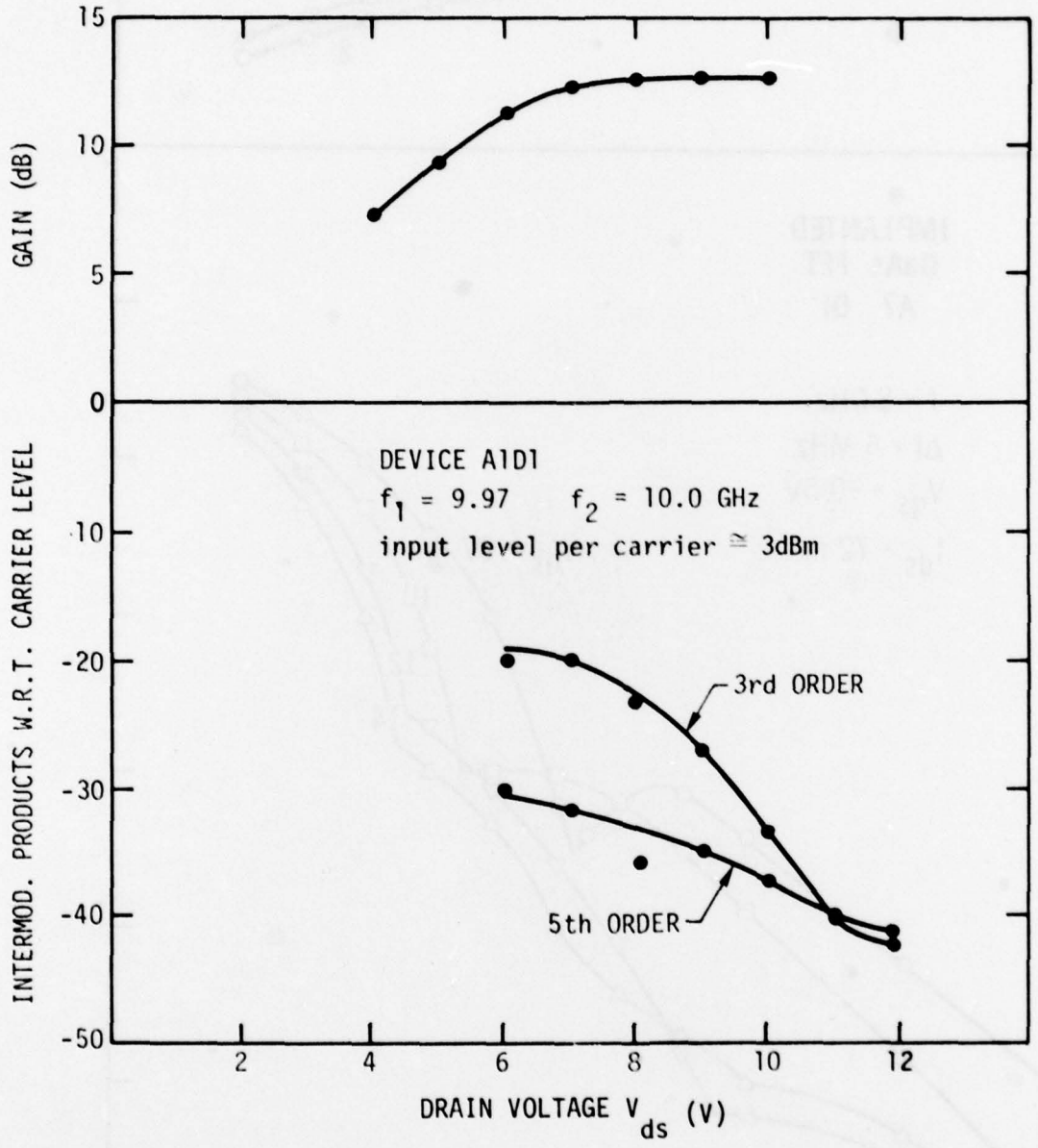

Fig. 4-6 Measured variation in gain and intermodulation products with drain voltage for Se implanted GaAs FET at 10 GHz.

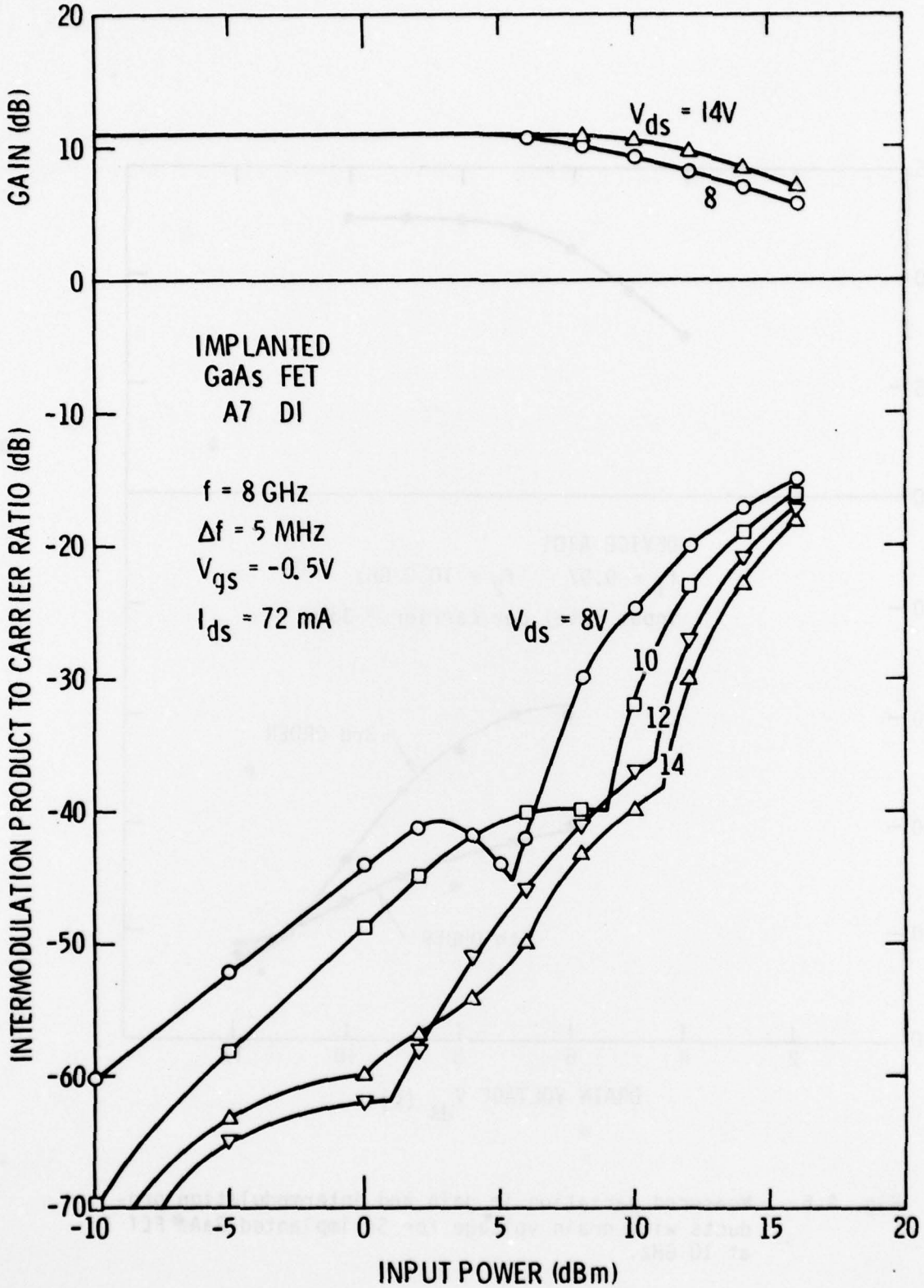

Fig. 4-7 Measured gain and third order intermodulation product vs input power for Se+Be implanted GaAs FET at 8 GHz with the drain voltage as a parameter.

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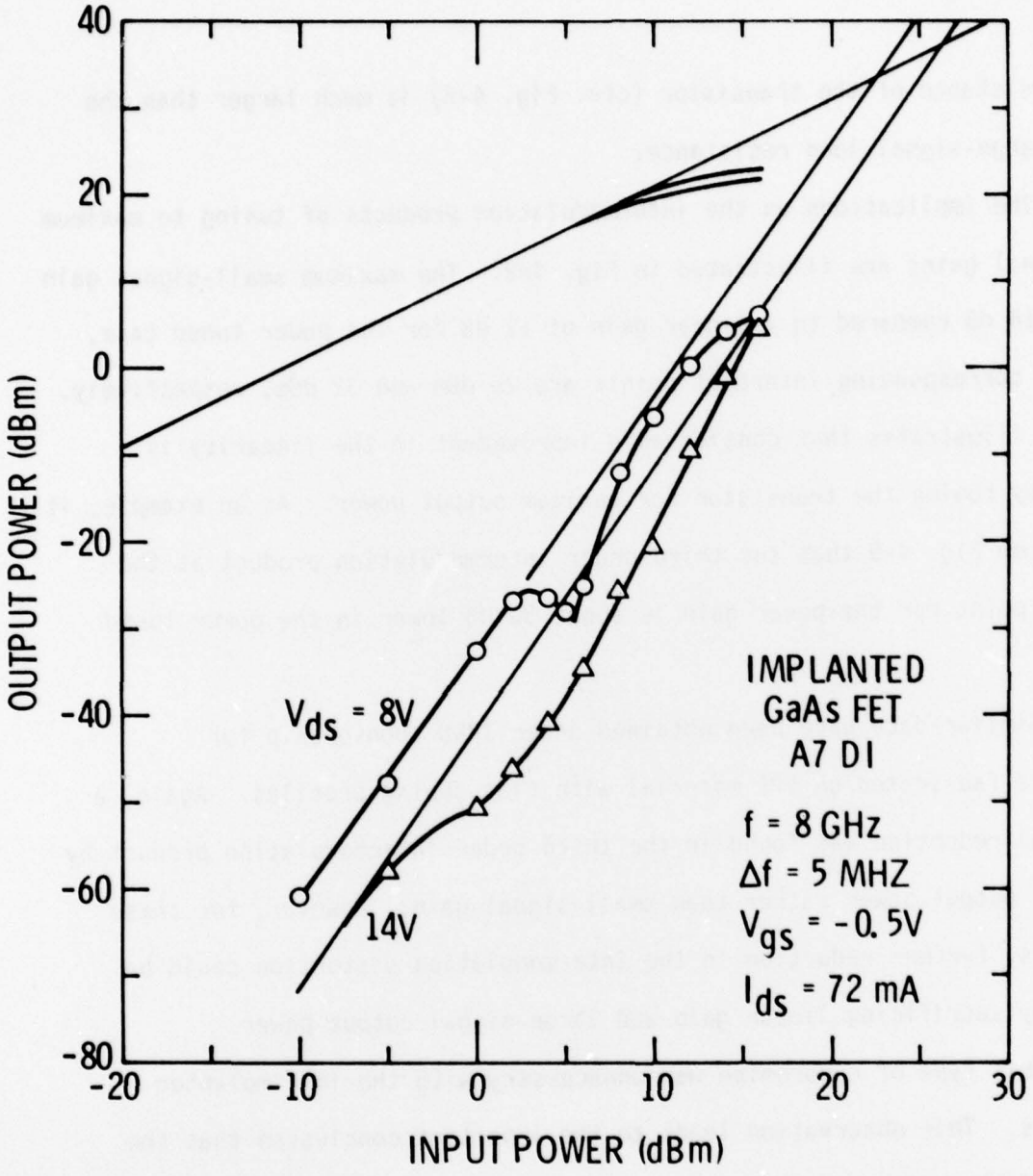

Fig. 4-8 Measured output power and third order intermodulation product vs input power for Se+Be implanted GaAs FET at 8 GHz with the drain voltage as a parameter.

output resistance of the transistor (cfr. Fig. 4-2) is much larger than the optimum large-signal load resistance.

The implications on the intermodulation products of tuning to maximum small-signal gains are illustrated in Fig. 4-9. The maximum small-signal gain is about 18 dB compared to a linear gain of 11 dB for the power tuned case, while the corresponding intercept points are 25 dBm and 32 dBm, respectively. This data illustrates that considerable improvement in the linearity is obtained by tuning the transistor for maximum output power. As an example, it is seen from Fig. 4-9 that the third order intermodulation product at the crossover point for the power gain is about 30 dB lower in the power tuned case.

Similar data have been obtained under IR&D sponsorship for transistors fabricated on VPE material with flat doping profiles. Again, a substantial reduction was found in the third order intermodulation product by tuning for output power rather than small-signal gain. However, for these transistors, further reduction in the intermodulation distortion could be obtained by sacrificing linear gain and large-signal output power.

This type of compromise was unnecessary with the ion implanted transistors. This observation leads to the important conclusion that the tuning conditions for optimum output power and minimum intermodulation distortion are virtually identical for optimized profiles (i.e. ion implanted Se+Be profiles) in contrast to conventional transistors with flat doping profiles.

A quantitative measure of the distortion advantage due to the improved tuning and transconductance characteristics of transistors with

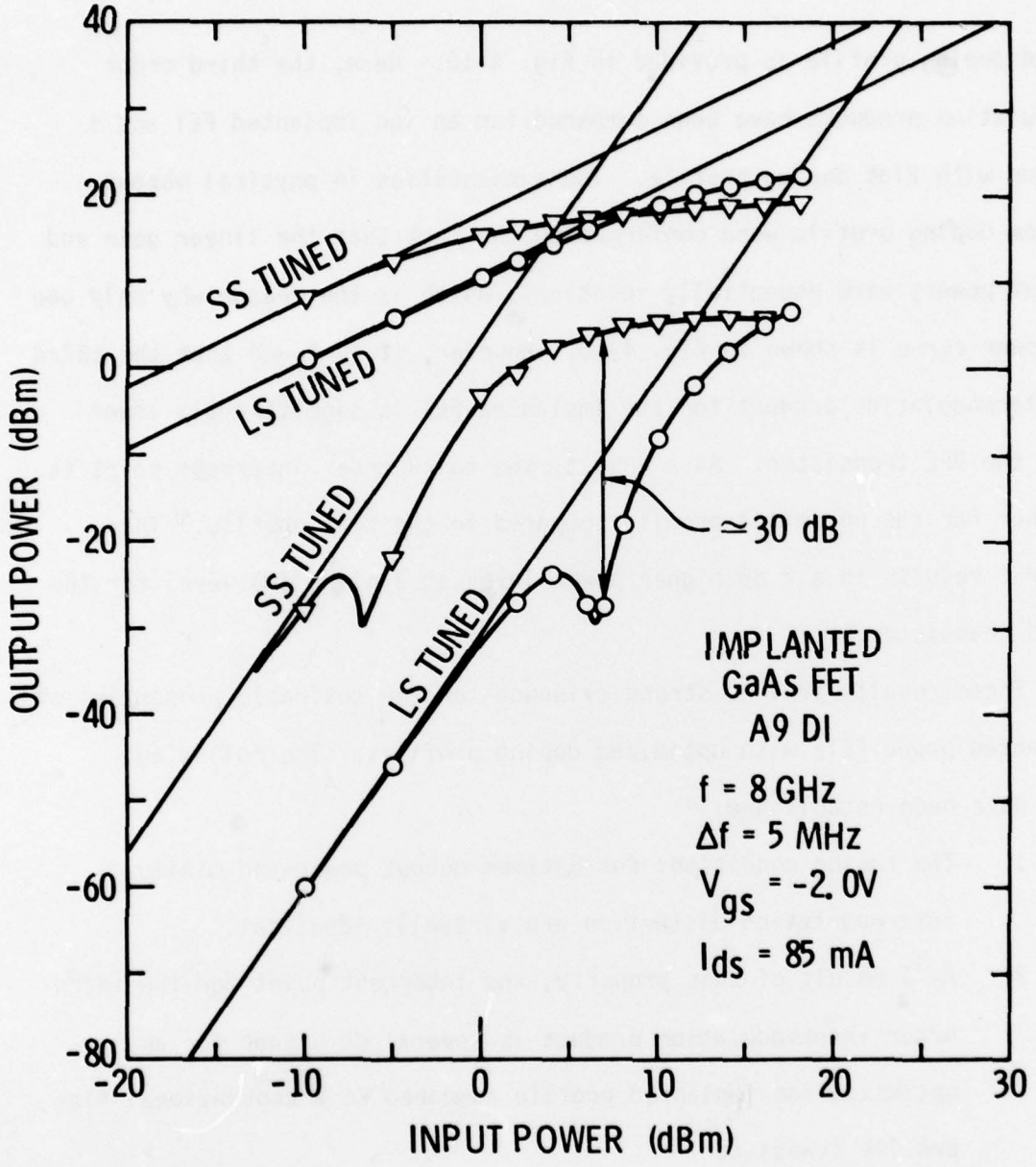

Fig. 4-9 Measured output power and third order intermodulation product vs input power for Se implanted GaAs FET at 8 GHz for tuning conditions of maximum linear gain and maximum output power.

optimized doping profile is provided in Fig. 4-10. Here, the third order intermodulation products have been compared for an ion implanted FET and a transistor with flat doping profile. The similarities in physical makeup aside from doping profile were confirmed by the fact that the linear gain and the output powers were essentially identical, which is the reason why only one output power curve is shown in Fig. 4-10. However, it is found that the third order intermodulation product for the implanted FET is significantly lower than for the VPE transistor. As a result, the third order intercept point is 4 dB higher for the optimized profile compared to the flat profile. This improvement results in a 2 dB higher power level at a given IMD level for the optimized transistor.

These results provide strong evidence for the desirable properties of ion implanted power FETs with optimized doping profiles. The following benefits have been established:

1. The tuning conditions for optimum output power and minimum intermodulation distortion are virtually identical.
2. As a result of this property, the intercept point for the third order intermodulation product is several dB higher for an optimized ion implanted profile compared to a conventional flat profile transistor.

The potential of the implanted Se+Be transistors as a power source was evaluated by measuring the output power at 7 GHz with a single-frequency input. An output power of 0.45W or 0.5W/mm was measured at a drain voltage of 15V. The associated gain was 5 dB. A significant increase in this result is expected by increasing the nt-product of the active layer.

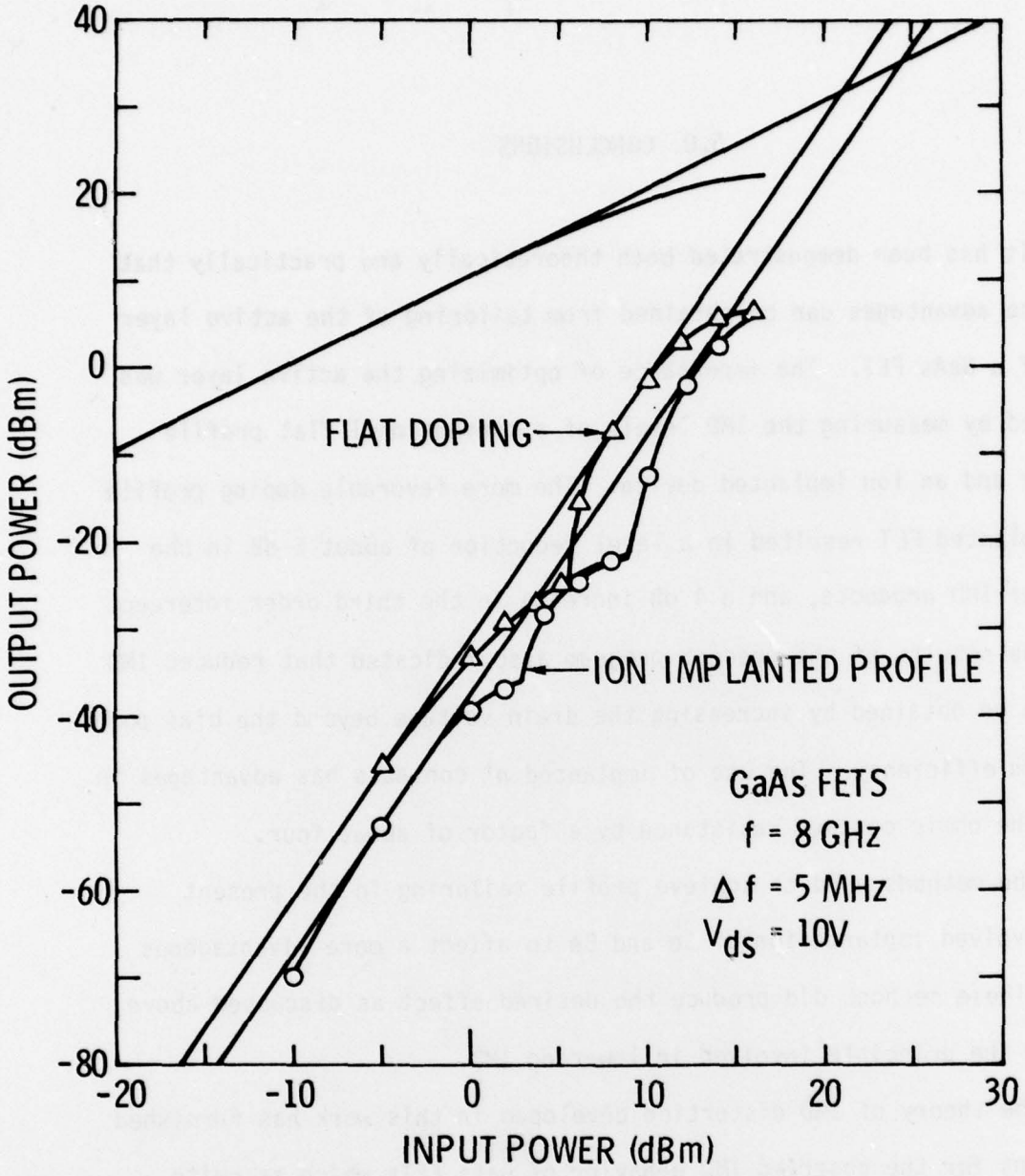

Fig. 4-10 Comparison of measured output power and third order intermodulation products vs input power at 8 GHz for conventional epitaxial FET with flat doping and Se+Be implanted FET.

5.0 CONCLUSIONS

It has been demonstrated both theoretically and practically that performance advantages can be obtained from tailoring of the active layer profile of a GaAs FET. The importance of optimizing the active layer was highlighted by measuring the IMD levels of a conventional flat profile transistor and an ion implanted device. The more favorable doping profile of the implanted FET resulted in a level reduction of about 6 dB in the third order IMD products, and a 4 dB increase in the third order intercept point. The results of the present program also indicated that reduced IMD levels can be obtained by increasing the drain voltage beyond the bias point for maximum efficiency. The use of implanted n^+ contacts has advantages in reducing the ohmic contact resistance by a factor of about four.

The methods used to achieve profile tailoring in the present program involved implantation of Se and Be to affect a more advantageous profile. These methods did produce the desired effect as discussed above and proved the principle involved in lowering IMD.

The theory of IMD distortion developed in this work has furnished explanations for the observed IMD behavior of GaAs FETs which is quite irregular in nature. Further work along these lines are expected to provide the necessary guidelines for obtaining transistors with optimum doping profiles.

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